A8.6.47 F* (former VFP instruction mnemonics)

Table A8-2 lists the UAL equivalents of pre-UAL VFP instruction mnemonics.

Table A8-2 VFP instruction mnemonics

Former ARM assembler mnemonic	UAL equivalent	See
FABSD, FABSS	VABS	*VABS* on page A8-532
FADDD, FADDS	VADD	*VADD (floating-point)* on page A8-538
FCMP, FCMPE, FCMPEZ, FCMPZ	VCMP{E}	*VCMP, VCMPE* on page A8-572
FCONSTD, FCONSTS	VMOV	*VMOV (immediate)* on page A8-640
FCPYD, FCPYS	VMOV	*VMOV (register)* on page A8-642
FCVTDS, FCVTSD	VCVT	*VCVT (between double-precision and single-precision)* on page A8-584
FDIVD, FDIVS	VDIV	*VDIV* on page A8-590
FLDD	VLDR	*VLDR* on page A8-628
FLDMD, FLDMS	VLDM, VPOP	*VLDM* on page A8-626. *VPOP* on page A8-694
FLDMX	FLDMX	*FLDMX, FSTMX* on page A8-101
FLDS	VLDR	*VLDR* on page A8-628
FMACD, FMACS	VMLA	*VMLA, VMLS (floating-point)* on page A8-636
FMDHR, FMDLR	VMOV	*VMOV (ARM core register to scalar)* on page A8-644
FMDRR	VMOV	*VMOV (between two ARM core registers and a doubleword extension register)* on page A8-652
FMRDH, FMRDL	VMOV	*VMOV (scalar to ARM core register)* on page A8-646
FMRRD	VMOV	*VMOV (between two ARM core registers and a doubleword extension register)* on page A8-652
FMRRS	VMOV	*VMOV (between two ARM core registers and two single-precision registers)* on page A8-650
FMRS	VMOV	*VMOV (between ARM core register and single-precision register)* on page A8-648
FMRX	VMRS	*VMRS* on page A8-658
FMSCD, FMSCS	VNMLS	*VNMLA, VNMLS, VNMUL* on page A8-674
FMSR	VMOV	*VMOV (between ARM core register and single-precision register)* on page A8-648
FMSRR	VMOV	*VMOV (between two ARM core registers and two single-precision registers)* on page A8-650
FMSTAT	VMRS	*VMRS* on page A8-658
FMULD, FMULS	VMUL	*VMUL (floating-point)* on page A8-664
FMXR	VMSR	*VMSR* on page A8-660

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Table A8-2 VFP instruction mnemonics (continued)

Former ARM assembler mnemonic	UAL equivalent	See
`FNEGD`, `FNEGS`	`VNEG`	*VNEG* on page A8-672
`FNMACD`, `FNMACS`	`VMLS`	*VMLA, VMLS (floating-point)* on page A8-636
`FNMSCD`, `FNMSCS`	`VNMLA`	*VNMLA, VNMLS, VNMUL* on page A8-674
`FNMULD`, `FNMULS`	`VNMUL`	*VNMLA, VNMLS, VNMUL* on page A8-674
`FSHTOD`, `FSHTOS`	`VCVT`	*VCVT (between floating-point and fixed-point, VFP)* on page A8-582
`FSITOD`, `FSITOS`	`VCVT`	*VCVT, VCVTR (between floating-point and integer, VFP)* on page A8-578
`FSLTOD`, `FSLTOS`	`VCVT`	*VCVT (between floating-point and fixed-point, VFP)* on page A8-582
`FSQRTD`, `FSQRTS`	`VSQRT`	*VSQRT* on page A8-762
`FSTD`	`VSTR`	*VSTR* on page A8-786
`FSTMD`, `FSTMS`	`VSTM`, `VPUSH`	*VSTM* on page A8-784, *VPUSH* on page A8-696
`FSTMX`	`FSTMX`	*FLDMX, FSTMX*
`FSTS`	`VSTR`	*VSTR* on page A8-786
`FSUBD`, `FSUBS`	`VSUB`	*VSUB (floating-point)* on page A8-790
`FTOSHD`, `FTOSHS`	`VCVT`	*VCVT (between floating-point and fixed-point, VFP)* on page A8-582
`FTOSI{Z}D`, `FTOSI{Z}S`	`VCVT{R}`	*VCVT, VCVTR (between floating-point and integer, VFP)* on page A8-578
`FTOSL`, `FTOUH`	`VCVT`	*VCVT (between floating-point and fixed-point, VFP)* on page A8-582
`FTOUI{Z}D`, `FTOUI{Z}S`	`VCVT{R}`	*VCVT, VCVTR (between floating-point and integer, VFP)* on page A8-578
`FTOULD`, `FTOULS`, `FUHTOD`, `FUHTOS`	`VCVT`	*VCVT (between floating-point and fixed-point, VFP)* on page A8-582
`FUITOD`, `FUITOS`	`VCVT`	*VCVT, VCVTR (between floating-point and integer, VFP)* on page A8-578
`FULTOD`, `FULTOS`	`VCVT`	*VCVT (between floating-point and fixed-point, VFP)* on page A8-582

FLDMX, FSTMX

Encodings T1/A1 of the `VLDM`, `VPOP`, `VPUSH`, and `VSTM` instructions contain an imm8 field that is set to twice the number of doubleword registers to be transferred. Use of these encodings with an odd value in imm8 is deprecated, and there is no UAL syntax for them.

The pre-UAL mnemonics `FLDMX` and `FSTMX` result in the same instructions as `FLDMD` (`VLDM.64` or `VPOP.64`) and `FSTMD` (`VSTM.64` or `VPUSH.64`) respectively, except that imm8 is equal to twice the number of doubleword registers plus one. Use of `FLDMX` and `FSTMX` is deprecated from ARMv6, except for disassembly purposes, and reassembly of disassembled code.

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