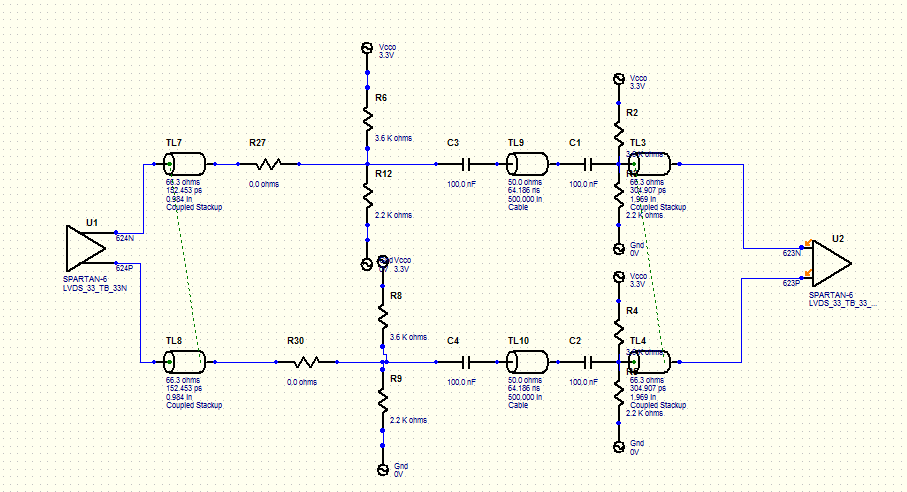
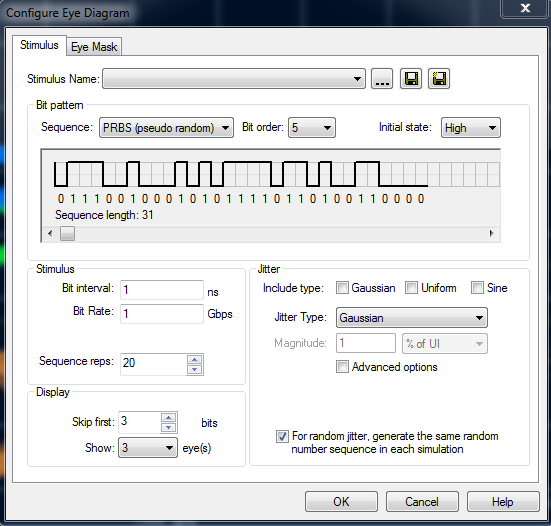
Circuit 1

Unidirectional link – no other pins connected (model does simulate effect of internal receiver in the IOB for the TX i.e. representative of how 2-pin bi-dir LVDS would look like)

Cable model is 50ohm cable @50inches (consistent for both scenario’s so ok for comparative sims)



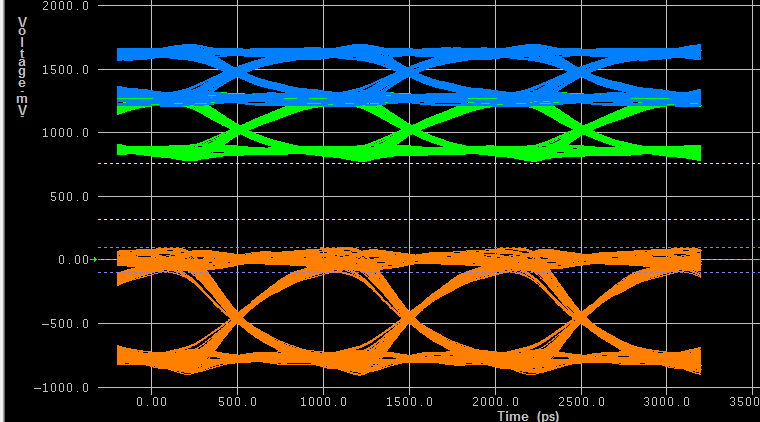
Sim settings

****

1000Mbps

Eye Height: 597mV

Eye Width: 846ps (of 1000ps) 85%

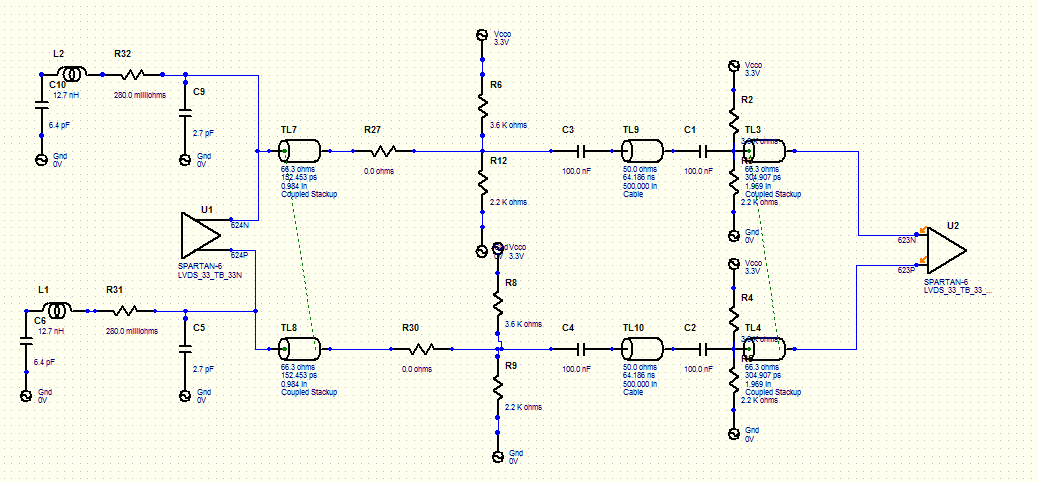
****

**Circuit 2**

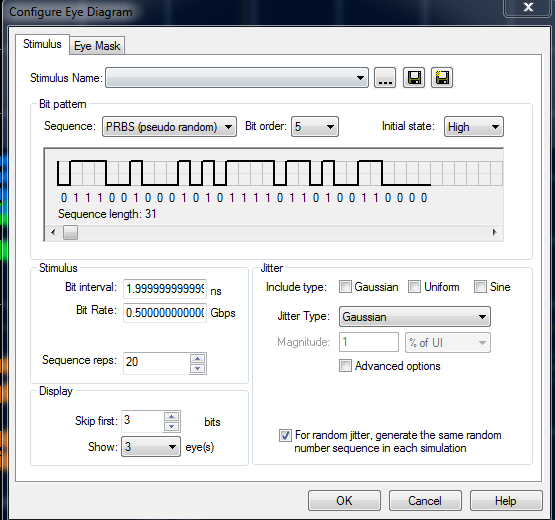
Simulating the effect of tying another set of pins to transmitter (emulates RX for other direction) . RX IO in tri-state.

Each pin has CRLC network (pulled from S6 model for FGG484 pkg)

Eg C10 -> C\_comp , L2 -> L\_pkg, R32 -> R\_pkg, C9 -> C-pkg



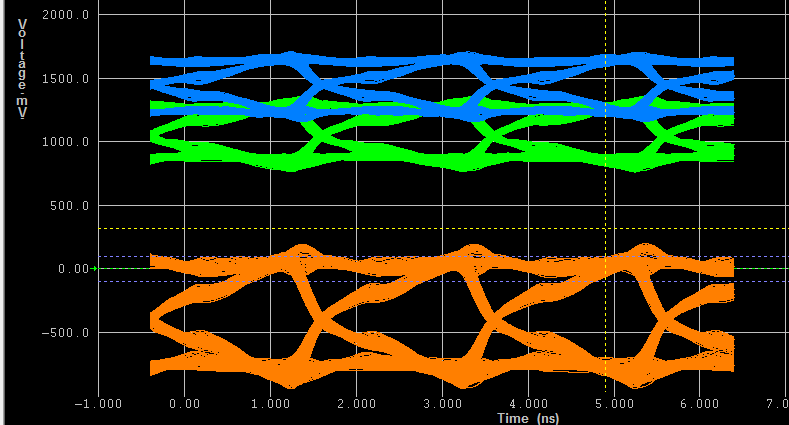
Sim settings



500Mbps

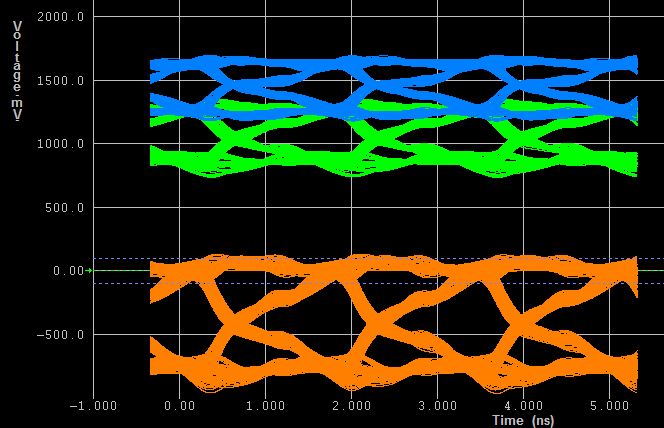
Eye Height: 440mV

Eye Width: 1779ps (of 2000ps) 88%



600Mbps

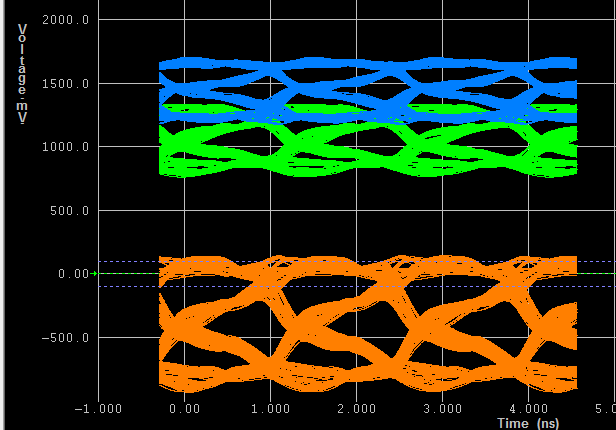
Eye Height: 405mV

Eye Width: 1254ps (of 1666ps) 75%

700Mbps

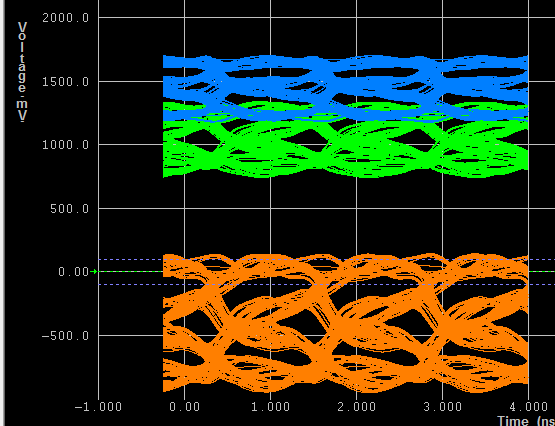
Eye Height: 269mV

Eye Width: 835ps (of 1428ps) 58%



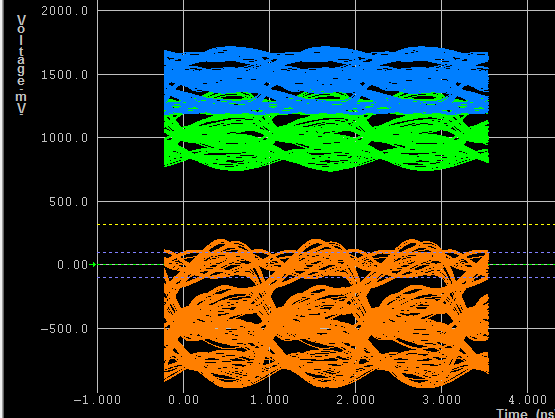
800Mbps

Eye Height: 143mV

Eye Width: 508ps (of 1025ps) 49.5%

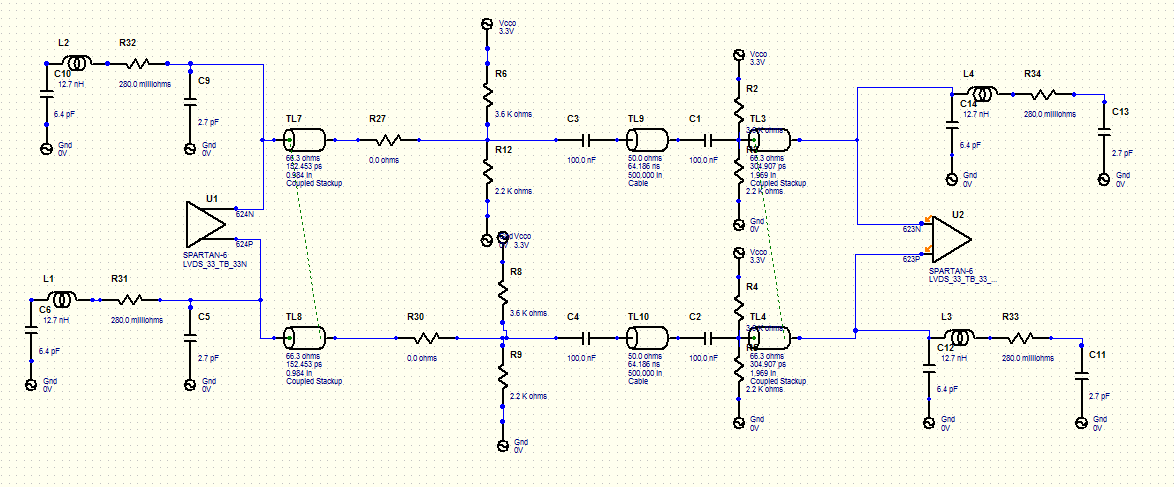
900Mbps

**Eye closed!**



**Circuit 3**

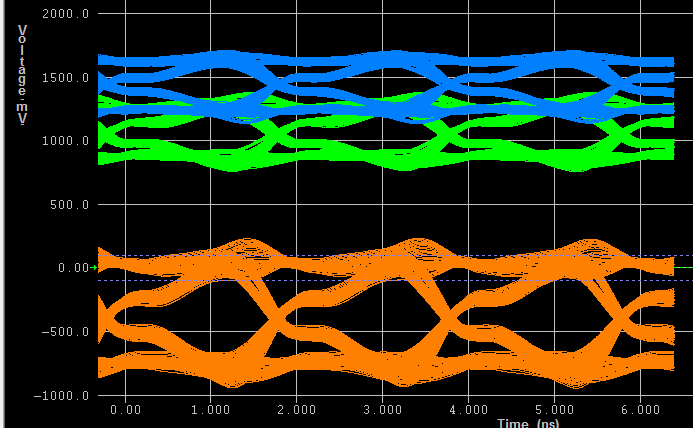
Adding same at RX end to emulate our system accurately

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500Mbps

Eye Height: 421mV

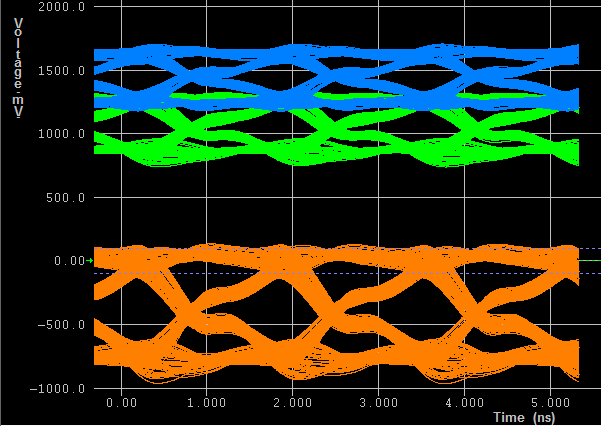
Eye Width: 1791ps (of 2000ps) 90%



600Mbps

Eye Height: 320mV

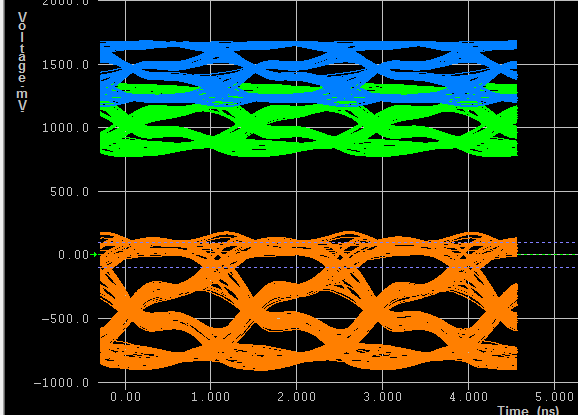
Eye Width: 1302ps (of 1666ps) 78%



700Mbps

Eye Height: 195mV

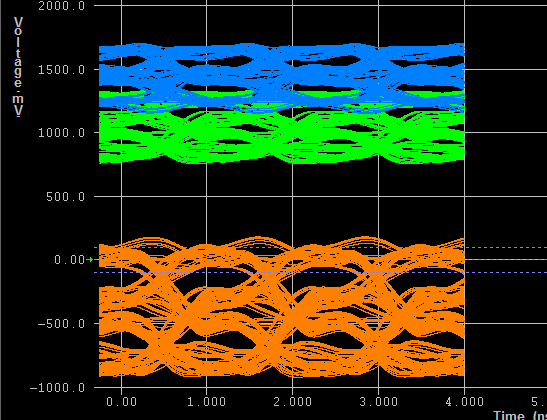
Eye Width: 935ps (of 1428ps) 65%

****

800Mbps

Eye Height: 39mV

Eye Width: 308ps (of 1025ps) 30%

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**Results Summary**



Table below shows Eye height/width versus datarate when modelled **with** extra pins