## Interrupts

*Table 12.3. Some of the TM4C NVIC interrupt enable registers. There are five such registers defining 139 interrupt enable bits.*

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Address | 31 | 30 | 29-7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Name |
| 0xE000E100 | G | F | … | UART1 | UART0 | E | D | C | B | A | NVIC\_EN0\_R |
| 0xE000E104 |   |   | … |   |   |   |   |   | UART2 | H | NVIC\_EN1\_R |

Calculating interrupt registers:

Each interrupt has an interrupt number and an IRQ number. Let x be the interrupt number and let n be the IRQ number. The interrupt number is

    x = n+16

The interrupt number defines the position in the vector table. The vector address is

    4\*x.

For example SysTick is interrupt number 15 and IRQ number -1.  Therefore the SysTick vector is at memory location 60, which is ROM location 0x0000003C.

For those interrupts with IRQ numbers greater and or equal to 0, we can find its priority register by dividingn by 4. Let m = n/4 (integer divide). The priority register number will be m. We can find the bit field for that IRQ by looking the remainder, p = n%4, where p = 0, 1, 2, or 3. The three bits will be 8\*p+7, 8\*p+6, and 8\*p+5.

|  |  |  |
| --- | --- | --- |
| p | Bit Field | Interrupt |
| 3 | Bits 31:29 | Interrupt [4m+3] |
| 2 | Bits 23:21 | Interrupt [4m+2] |
| 1 | Bits 15:13 | Interrupt [4m+1] |
| 0 | Bits 7:5 | Interrupt [4m] |

For example, Timer3A is interrupt number 51 and IRQ number 35. n=35, so m=35/4 = 8. p=35%4=3. So the Timer3A priority register is 8 (NVIC\_PRI8\_R), and the three priority bits are be 8\*3+7, 8\*3+6, and 8\*3+5, which are 31, 30, and 29.

For those interrupts with IRQ numbers greater and or equal to 0, we can find its enable register by dividing nby 32. Let a = n/32 (integer divide). The enable register number will be a. We can find the bit field for that IRQ by looking the remainder, b = n%32, where b = 0, 1, ... or 31. The one bit will be used to enable the interrupt.

Again, Timer3A is interrupt number 51 and IRQ number 35. n=35, so a=35/32 = 1. b=35%32=3. So the Timer3A enable register is 1 (NVIC\_EN1\_R), and the enable bit is bit 3.