1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
<REV>	<ECN>	<ECO_DESCRIPTION>	<ECODATE>

X260 MLB - CBB

LAST_MODIFICATION=Thu Sep 10 15:22:41 2015

PAGE	<CSA>	CONTENTS	SYNC	DATE
1	1	page1	MASTER	MASTER
2	2	page2	J43_MLB	10/24/2012
3	3	page3	J43_MLB	10/24/2012
4	4	page4	J43_MLB	10/24/2012
5	5	page5	DEVMLB	05/11/2015
6	6	page6	DEVMLB	05/11/2015
7	7	page7	DEVMLB	04/14/2015
8	8	page8	DEVMLB	05/11/2015
9	9	page9	DEVMLB	05/11/2015
10	10	page10	DEVMLB	04/14/2015
11	11	page11	DEVMLB	04/14/2015
12	12	page12	DEVMLB	05/06/2015
13	13	page13	DEVMLB	05/11/2015
14	14	page14	DEVMLB	05/11/2015
15	15	page15	DEVMLB	05/11/2015
16	16	page16	DEVMLB	05/11/2015
17	17	page17	DEVMLB	05/11/2015
18	19	page19	DEVMLB	05/11/2015
19	20	page20	DEVMLB	05/04/2015
20	22	page22	DEVMLB	04/14/2015
21	23	page23	DEVMLB	04/14/2015
22	25	page25	DEVMLB	04/14/2015
23	30	page30	DEVMLB	04/09/2015
24	31	page31	DEVMLB	05/11/2015
25	37	page37	J72_MLB	05/13/2015
26	38	page38	J92_DEVMLB	05/13/2015
27	39	page39	DEVMLB	04/14/2015
28	40	page40	DEVMLB	04/14/2015
29	48	page48	DEVMLB	05/11/2015
30	50	page50	DEVMLB	05/11/2015
31	51	page51	DEVMLB	04/14/2015
32	52	page52	DEVMLB	04/14/2015
33	53	page53	DEVMLB	05/11/2015
34	54	page54	DEVMLB	05/11/2015
35	55	page55	DEVMLB	03/16/2015
36	61	page61	J92_DEVMLB	07/23/2013
37	62	page63	DEVMLB	05/11/2015
38	63	page64	DEVMLB	05/11/2015
39	64	page67	DEVMLB	05/11/2015
40	67	page69	DEVMLB	03/16/2015
41	69	page70	<SYNC_MASTER41>	03/16/2015
42	70	page71	DEVMLB	05/11/2015
43	71	page72	DEVMLB	05/06/2015
44	72	page74	DEVMLB	05/11/2015
45	74	page76	DEVMLB	05/11/2015

PAGE	<CSA>	CONTENTS	SYNC	DATE
46	76	page78	DEVMLB	05/13/2015
47	78	page79	DEVMLB	05/11/2015
48	79	page80	DEVMLB	05/11/2015
49	80	page81	DEVMLB	05/11/2015
50	81	page82	DEVMLB	04/30/2015
51	82	page83	DEVMLB	05/06/2015
52	83	page84	DEVMLB	05/11/2015
53	84	page85	DEVMLB	03/16/2015
54	85	page86	DEVMLB	05/11/2015
55	86	page87	DEVMLB	05/13/2015
56	87	page88	DEVMLB	05/11/2015
57	88	page90	DEVMLB	05/11/2015
58	90	page91	DEVMLB	05/11/2015
59	91	page93	DEVMLB	05/13/2015
60	93	page96	DEVMLB	05/13/2015
61	96	page100	DEVMLB	03/16/2015
62	100	page102	J43_MLB	10/24/2012
63	102	page103	DEVMLB	04/30/2015
64	103	page104	J92_DEVMLB	07/08/2014
65	104	page105	J92_DEVMLB	07/08/2014
66	105	page120	J41_MLB	10/24/2012
67	120	page130	J92_LAYOUT_STUDY_MLB	05/18/2015
	130		MASTER	MASTER
	<CSA_PAGE69>		<SYNC_MASTER69>	<SYNC_DATE69>
	<CSA_PAGE70>		<SYNC_MASTER70>	<SYNC_DATE70>
	<CSA_PAGE71>		<SYNC_MASTER71>	<SYNC_DATE71>
	<CSA_PAGE72>		<SYNC_MASTER72>	<SYNC_DATE72>
	<CSA_PAGE73>		<SYNC_MASTER73>	<SYNC_DATE73>
	<CSA_PAGE74>		<SYNC_MASTER74>	<SYNC_DATE74>
	<CSA_PAGE75>		<SYNC_MASTER75>	<SYNC_DATE75>
	<CSA_PAGE76>		<SYNC_MASTER76>	<SYNC_DATE76>
	<CSA_PAGE77>		<SYNC_MASTER77>	<SYNC_DATE77>
	<CSA_PAGE78>		<SYNC_MASTER78>	<SYNC_DATE78>
	<CSA_PAGE79>		<SYNC_MASTER79>	<SYNC_DATE79>
	<CSA_PAGE80>		<SYNC_MASTER80>	<SYNC_DATE80>
	<CSA_PAGE81>		<SYNC_MASTER81>	<SYNC_DATE81>
	<CSA_PAGE82>		<SYNC_MASTER82>	<SYNC_DATE82>
	<CSA_PAGE83>		<SYNC_MASTER83>	<SYNC_DATE83>
	<CSA_PAGE84>		<SYNC_MASTER84>	<SYNC_DATE84>
	<CSA_PAGE85>		<SYNC_MASTER85>	<SYNC_DATE85>
	<CSA_PAGE86>		<SYNC_MASTER86>	<SYNC_DATE86>
	<CSA_PAGE87>		<SYNC_MASTER87>	<SYNC_DATE87>
	<CSA_PAGE88>		<SYNC_MASTER88>	<SYNC_DATE88>
	<CSA_PAGE89>		<SYNC_MASTER89>	<SYNC_DATE89>
	<CSA_PAGE90>		<SYNC_MASTER90>	<SYNC_DATE90>

ALIASES RESOLVED

Table of Contents [1]

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-00532	1	SCHEM,MLB,X260	SCH	CRITICAL	
820-00244	1	PCBF,MLB,X260	PCB	CRITICAL	

PRODUCT SAFETY REQUIREMENTS:
PCB, UL RECOGNIZED, MIN. 130-C TEMP. RATING AND V-0 FLAME RATING PER UL 796 & UL 94.
PCB TO BE SILK-SCREENED WITH UL/CUL RECOGNITION MARK, MANUFACTURER'S UL FILE NUMBER, UL PCB MATERIAL DESIGNATION, 130-C TEMP. RATING AND V-0 FLAME RATING.

DRAWING TITLE: <PART_DESCRIPTION>

Apple Inc.

DRAWING NUMBER: <SCH_NUM> | SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 1 OF 130
SHEET: 1 OF 67

BOM Groups

BOM GROUP	BOM OPTIONS
MLB_COMMON	ALTERNATE,COMMON,MLB_MISC,MLB_DEBUG:ENG,MLB_PROGPARTS,BUILD:CBB
MLB_MISC	CAM_FREQ:24M,CAM_XTAL:NO,SSDRAM:4GBIT,S3X:B0,UPC:A1,PCH24M:SUS,EQ:4CH,PMIC:A0D,BSSB_GPIO
MLB_DEBUG:ENG	DEBUGLED

CPU DRAM SPD Straps

BOM GROUP	BOM OPTIONS
DRAM:SAM_8GB	RAMCFG0_L,DRAM_TYPE:SAMSUNG_8GB
DRAM:HYN_8GB	RAMCFG0_L,RAMCFG1_L,DRAM_TYPE:HYNIX_8GB
DRAM:ELP_8GB	DRAM_TYPE:ELPIDA_8GB

CPU DRAM CFG Chart

VENDOR	CFG 1	CFG 0
HYNIX	0	0
SAMSUNG	1	0
MICRON	0	1
ELPIDA	1	1

SIZE	CFG 3	CFG 2
2GB	0	0
4GB QDP	0	1
4GB DDP	1	0
8GB	1	1

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S00074	376S0855		ALL	Toshiba alt for Diodes dual
376S1129	376S0855		ALL	NXP alt for Diodes dual
376S1089	376S1128		ALL	NXP alt for Diodes single
138S0703	138S0648		ALL	Murata alt to Taiyo Yuden
372S0186	372S0185		ALL	NXP alt to Diodes
376S1053	376S0604		ALL	Diodes alt to Fairchild
107S0249	107S0251		ALL	TFT alt to Cyntec
128S00044	128S00041		ALL	Rubycon alt to Sanyo
740S00004	740S0134		ALL	Kemet alt to Sanyo
740S00005	740S0190		ALL	Polytronics alt to Wayon
128S0296	128S0487		ALL	Sanyo alt to NEC
128S00012	128S0487		ALL	ROHM alt to NEC
128S0397	128S0325		ALL	Kemet alt to Sanyo
107S00070	107S0085		ALL	TDK alt to Murata
376S00007	376S1179		ALL	AOS alt to Vishay
376S1080	376S0820		ALL	Diodes alt to Onsemi
152S00311	152S2037		ALL	Cyntec new alt to Cyntec
152S00098	152S00224		ALL	Vishay alt to Cyntec
128S00021	128S00020		ALL	ROHM alt to NEC
138S0786	138S0705		ALL	Samsung alt to Murata

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S00007	128S00015		ALL	NEC alt to Sanyo
128S00009	128S00015		ALL	Kemet alt to Sanyo
128S00029	128S00015		ALL	Rohm alt to Sanyo
128S00011	128S00010		ALL	Kemet alt to Sanyo
128S00026	128S00010		ALL	NEC alt to Sanyo
128S00031	128S00010		ALL	Rohm alt to Sanyo
138S00073	138S00047		ALL	Murata alt to Taiyo
138S0772	138S00013		ALL	Taiyo alt to Murata
132S00012	132S0401		ALL	Multi alt to Taiyo
152S00028	152S1751		ALL	Murata alt to Taiyo Yuden
353S00712	353S2216		ALL	OnSemi alt to TI
353S00714	353S2208		ALL	ONSemi alt to TI
337S00174	337S00175	S3X:B0	ALL	S3X B0 alt to A0
138S00077	138S00035		ALL	Taiyo alt to Murata
152S00343	152S1682		ALL	Murata alt to Cyntec
155S00155	155S0441		ALL	TDK alt to Murata
155S0741	155S0361		ALL	Murata alt to TDK
155S00165	155S0382		ALL	Taiyo alt to TDK
155S00166	155S0391		ALL	TDK alt to Murata
155S0706	155S0302		ALL	Taiyo alt to Murata
197S00053	197S00050		ALL	Kyocera alt to TXC
197S00055	197S00050		ALL	Murata alt to TXC
311S00004	311S0370		ALL	OnSemi alt to NXP
333S00030	333S00016		ALL	Hynix alt to Micron
338S00175	338S1264		ALL	Broadcom alt packaging
107S00020	107S0276		ALL	TFT alt to Cyntec
107S00021	107S0284		ALL	TFT alt to Cyntec
353S00773	353S4296		ALL	Semtech alt to TI
311S00057	311S0612		ALL	Diodes alt to NXP
155S00011	155S00008		ALL	Murata alt to TDK
138S0739	138S0706		ALL	Samsung alt to Murata
138S0945	138S0706		ALL	Kyocera alt to Murata
138S00090	138S0943		ALL	Taiyo alt to Murata
138S00087	138S1086		ALL	Taiyo alt to Murata
107S00086	107S00056		ALL	TFT alt to Cyntec
152S00347	152S00220		ALL	Chilisin alt to Cyntec
138S00032	138S0831		ALL	Taiyo alt to Murata
138S00049	138S0831		ALL	Kyocera alt to Murata
152S00362	152S1129		ALL	Cyntec alt to Murata
128S00039	128S00038		ALL	NEC alt to Kemet

Programmable Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S00084	1	IC,SPI SERIAL FLASH,8MBIT,3.0V,CSP,8P	U3090	CRITICAL	UPCROM:BLANK
341S00466	1	IC,NVM (VXXX) CBB, X260	U3090	CRITICAL	UPCROM:PROG
338S1231	1	IC,SMC12-B1,40MHZ/50DMIPS MCU,7X7,168BGA	U5000	CRITICAL	SMC:BLANK
341S00431	1	IC,SMC-B1,EXTERNAL (V2.33A2) PROTO 1,X260	U5000	CRITICAL	SMC:PROG
335S1009	1	64 MBIT SPI QUAD I/O FLASH,CSP,3.3V,QUAD IO	U6100	CRITICAL	BOOTROM_WIN:BLANK
335S1010	1	64 MBIT SPI QUAD I/O FLASH,CSP,3.3V,QUAD IO	U6100	CRITICAL	BOOTROM_MAC:BLANK
335S1029	1	64 MBIT SPI QUAD I/O FLASH,CSP,3.3V,QUAD IO	U6100	CRITICAL	BOOTROM_MIC:BLANK
341S00465	1	IC,EFI ROM (VXXX) CBB,X260	U6100	CRITICAL	BOOTROM:PROG

SSD Configs

BOM GROUP	BOM OPTIONS
SSD:128GB	NAND:64GB,CAPACITY1
SSD:256GB	NAND:128GB,CAPACITY0,CAPACITY1
SSD:512GB	NAND:256GB,CAPACITY2
SSD:256GB_SAND	NAND:128GB_SAND,CAPACITY0,CAPACITY1,SANDISK_1Y
SSD:512GB_SAND	NAND:256GB_SAND,CAPACITY2,SANDISK_1Y

SSD Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S00175	1	IC,S3-X,B0	U8600	CRITICAL	S3X:B0
333S00017	1	IC,LPDDR3-1600,128MX8,1.8V,25NN,276 POP	U8600_POP_DRAM	CRITICAL	SSDRAM:4GBIT
335S1030	2	NAND,TOG DDR2,2CH,64GB,1YNM,3.3V,LGA60	U9100,U9120	CRITICAL	NAND:64GB
335S00050	2	NAND,TOG DDR2,2CH,128GB,1YNM,3.3V,LGA60	U9100,U9120	CRITICAL	NAND:128GB
335S00051	2	NAND,TOG DDR2,2CH,256GB,1YNM,3.3V,LGA60	U9100,U9120	CRITICAL	NAND:256GB
335S00121	2	NAND,TOG DDR2,2CH,128GB,1YNM,3.3V,LGA60	U9100,U9120	CRITICAL	NAND:128GB_SAND
335S00122	2	NAND,TOG DDR2,2CH,256GB,1YNM,3.3V,LGA60	U9100,U9120	CRITICAL	NAND:256GB_SAND

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S00207	1	IC,CPU,SKY,SR2EN,PBQ,D1,2/2,1.1,5W,.85,B1515	U0500	CRITICAL	CPU:1.1GHZ
337S00208	1	IC,CPU,SKY,SR2EM,PBQ,D1,2/2,1.2,5W,.85,B1515	U0500	CRITICAL	CPU:1.2GHZ
337S00209	1	IC,CPU,SKY,SR2EH,PBQ,D1,2/2,1.3,5W,.85,B1515	U0500	CRITICAL	CPU:1.3GHZ
946-3892	1	J11/J13 MLB DYMAX ADHESIVE 29993-SC 0.4G	GLUE	CRITICAL	
825-00162	1	LABEL,BARCODE,2D,1D,CONFIG,MLB,X260	LABEL		

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S00660	1	IC,CD3215,USB PWR SWITCH,A1,6X6MM,BGA96	U3100	CRITICAL	UPC:A1
338S00168	1	IC,PMU,P650839A0D,7X7MM,BGA168	U7800	CRITICAL	PMIC:A0D

Board IDs

BOM GROUP	BOM OPTIONS
BUILD:PROTO1	BOARDID0_L
BUILD:CBB	BOARDID1_L

Board ID should start all-high (first build), and each new build increment stuffing
in a binary fashion (ID0 is the LSb). IDx is high if not set low in the BOM table.

DRAM Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S00052	2	IC,SDRAM,LPDDR-1866,32GBIT,253B FBGA	U2300,U2500	CRITICAL	DRAM_TYPE:SAMSUNG_8GB
333S00053	2	IC,SDRAM,LPDDR-1866,32GBIT,253B FBGA	U2300,U2500	CRITICAL	DRAM_TYPE:HYNIX_8GB
333S00054	2	IC,SDRAM,LPDDR-1866,32GBIT,253B FBGA	U2300,U2500	CRITICAL	DRAM_TYPE:ELPIDA_8GB

SYNC_MASTER=X260_ERIC SYNC_DATE=06/09/2015

PAGE TITLE: BOM Configuration [2]

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 2 OF 130

SHEET: 2 OF 67

Top level BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
639-6664	PCBA,MLB,1.3GHZ,EL 8GB,TOSH 256G,WIFI FCC,X260	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,SSD:256GB,WIFI:FCC
639-6665	PCBA,MLB,1.3GHZ,EL 8GB,TOSH 512G,WIFI FCC,X260	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,SSD:512GB,WIFI:FCC
639-6666	PCBA,MLB,1.3GHZ,HY 8GB,TOSH 256G,WIFI FCC,X260	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:HYN_8GB,SSD:256GB,WIFI:FCC
639-6667	PCBA,MLB,1.3GHZ,HY 8GB,TOSH 512G,WIFI FCC,X260	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:HYN_8GB,SSD:512GB,WIFI:FCC
639-6668	PCBA,MLB,1.3GHZ,SA 8GB,TOSH 256G,WIFI FCC,X260	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:SAM_8GB,SSD:256GB,WIFI:FCC
639-6669	PCBA,MLB,1.3GHZ,SA 8GB,TOSH 512G,WIFI FCC,X260	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:SAM_8GB,SSD:512GB,WIFI:FCC
639-6670	PCBA,MLB,1.1GHZ,HY 8GB,TOSH 128G,WIFI FCC,X260	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:HYN_8GB,SSD:128GB,WIFI:FCC
639-6671	PCBA,MLB,1.2GHZ,EL 8GB,TOSH 256G,WIFI ETSI,X260	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,SSD:256GB,WIFI:ETSI
639-6672	PCBA,MLB,1.2GHZ,SA 8GB,TOSH 512G,WIFI APAC,X260	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:SAM_8GB,SSD:512GB,WIFI:APAC
639-6673	PCBA,MLB,1.2GHZ,EL 8GB,SAND 256G,WIFI ETSI,X260	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,SSD:256GB_SAND,WIFI:ETSI
639-6674	PCBA,MLB,1.3GHZ,EL 8GB,SAND 256G,WIFI FCC,X260	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,SSD:256GB_SAND,WIFI:FCC
639-6675	PCBA,MLB,1.3GHZ,SA 8GB,SAND 512G,WIFI APAC,X260	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:SAM_8GB,SSD:512GB_SAND,WIFI:APAC
639-6676	PCBA,MLB,1.2GHZ,EL 8GB,SAND 256G,WIFI FCC,X260	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,SSD:256GB_SAND,WIFI:FCC
639-6677	PCBA,MLB,1.3GHZ,SA 8GB,SAND 512G,WIFI FCC,X260	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:SAM_8GB,SSD:512GB_SAND,WIFI:FCC
639-6678	PCBA,MLB,1.3GHZ,HY 8GB,SAND 512G,WIFI FCC,X260	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:HYN_8GB,SSD:512GB_SAND,WIFI:FCC
639-6679	PCBA,MLB,1.2GHZ,HY 8GB,SAND 512G,WIFI FCC,X260	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:HYN_8GB,SSD:512GB_SAND,WIFI:FCC
639-6680	PCBA,MLB,1.1GHZ,HY 8GB,TOSH 512G,WIFI FCC,X260	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:HYN_8GB,SSD:512GB,WIFI:FCC
639-6681	PCBA,MLB,1.2GHZ,HY 8GB,TOSH 256G,WIFI FCC,X260	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:HYN_8GB,SSD:256GB,WIFI:FCC
639-6682	PCBA,MLB,1.2GHZ,SA 8GB,SAND 256G,WIFI FCC,X260	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:SAM_8GB,SSD:256GB_SAND,WIFI:FCC
639-6683	PCBA,MLB,1.3GHZ,SA 8GB,SAND 256G,WIFI FCC,X260	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:SAM_8GB,SSD:256GB_SAND,WIFI:FCC
639-6684	PCBA,MLB,1.1GHZ,SA 8GB,SAND 512G,WIFI ETSI,X260	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:SAM_8GB,SSD:512GB_SAND,WIFI:ETSI
639-6685	PCBA,MLB,1.2GHZ,SA 8GB,SAND 256G,WIFI IND,X260	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:SAM_8GB,SSD:256GB_SAND,WIFI:IND
639-6686	PCBA,MLB,1.3GHZ,HY 8GB,TOSH 128G,WIFI FCC,X260	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:HYN_8GB,SSD:128GB,WIFI:FCC
639-6687	PCBA,MLB,1.1GHZ,SA 8GB,TOSH 128G,WIFI FCC,X260	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:SAM_8GB,SSD:128GB,WIFI:FCC
639-6688	PCBA,MLB,1.1GHZ,HY 8GB,TOSH 256G,WIFI FCC,X260	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:HYN_8GB,SSD:256GB,WIFI:FCC
639-6689	PCBA,MLB,1.1GHZ,SA 8GB,SAND 256G,WIFI FCC,X260	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:SAM_8GB,SSD:256GB_SAND,WIFI:FCC
639-6690	PCBA,MLB,1.1GHZ,SA 8GB,SAND 512G,WIFI FCC,X260	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:SAM_8GB,SSD:512GB_SAND,WIFI:FCC
639-6691	PCBA,MLB,1.2GHZ,HY 8GB,TOSH 128G,WIFI FCC,X260	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:HYN_8GB,SSD:128GB,WIFI:FCC
639-6692	PCBA,MLB,1.2GHZ,SA 8GB,TOSH 128G,WIFI FCC,X260	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:SAM_8GB,SSD:128GB,WIFI:FCC
639-6693	PCBA,MLB,1.2GHZ,SA 8GB,TOSH 512G,WIFI FCC,X260	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:SAM_8GB,SSD:512GB,WIFI:FCC
639-6694	PCBA,MLB,1.3GHZ,SA 8GB,TOSH 128G,WIFI FCC,X260	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:SAM_8GB,SSD:128GB,WIFI:FCC

Partial & development BOMs

BOM NUMBER	BOM NAME	BOM OPTIONS
685-00073	CMN PTS,PCBA,MLB,X260	MLB_COMMON
939-01879	PCBA,MLB,NO CPU,SA 8GB,TOSH 512G,WIFI FCC,X260	ALTERNATE,CMN,DRAM:SAM_8GB,SSD:512GB,WIFI:FCC
939-01880	PCBA,MLB,NO CPU,SA 8GB,SAND 512G,WIFI FCC,X260	ALTERNATE,CMN,DRAM:SAM_8GB,SSD:512GB_SAND,WIFI:FCC

BOM Groups

BOM GROUP	BOM OPTIONS
MLB_PROGPARTS	BOOTROM:PROG,BT:PROG,SMC:PROG,UPCROM:PROG

Common BOM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
685-00073	1	CMN PTS,PCBA,MLB,X260	CMNPTS	CRITICAL	CMN

Programmable Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
341S00345	1	BT ROM (VXX) PROTO0,X260	U3770	CRITICAL	BT:PROG
341S00346	1	WIFI ROM (PXXXX) PROTO0,WW1,X260	U3780	CRITICAL	WIFI:FCC
341S00347	1	WIFI ROM (PXXXX) PROTO0,WW2,X260	U3780	CRITICAL	WIFI:ETSI
341S00348	1	WIFI ROM (PXXXX) PROTO0,WW3,X260	U3780	CRITICAL	WIFI:APAC
341S00349	1	WIFI ROM (PXXXX) PROTO0,IND,X260	U3780	CRITICAL	WIFI:IND

SYNC_MASTER=J43_MLB SYNC_DATE=10/24/2012

PAGE TITLE

X260 BOM Variants

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

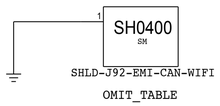
REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 3 OF 130

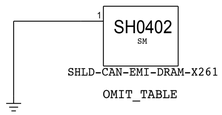
SHEET 3 OF 67

WIFI EMI CAN



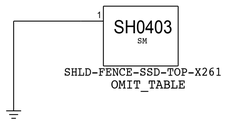
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
806-7064	1	CAN,EMI,WIFI,X261	SH0400	CRITICAL	

DRAM EMI CAN

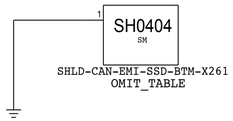


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
806-04848	1	CAN,EMI,DRAM,X260	SH0402	CRITICAL	

SSD EMI CANs

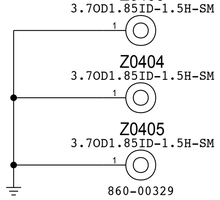


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
806-00889	1	FENCE,EMI,SSD,TOP,X261	SH0403	CRITICAL	
870-00878	1	TAPE,CONDUCTIVE,SSD,REEL,X261	SSD_TAPE_TOP	CRITICAL	

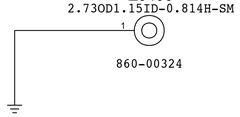


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
806-05622	1	FENCE,EMI,SSD,BTM,X260	SH0404	CRITICAL	
870-01557	1	TAPE,CONDUCTIVE,SSD,REEL,X260	SSD_TAPE_BTM	CRITICAL	

CPU Heat Spreader Bosses



USB-C BTB Connector Boss



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
870-00998	1	MYLAR,SHIM,MLB,X261	MYLAR_SHIM	CRITICAL	

SYNC_MASTER=J43_MLB SYNC_DATE=10/24/2012

PAGE TITLE

PD PARTS

Apple Inc.

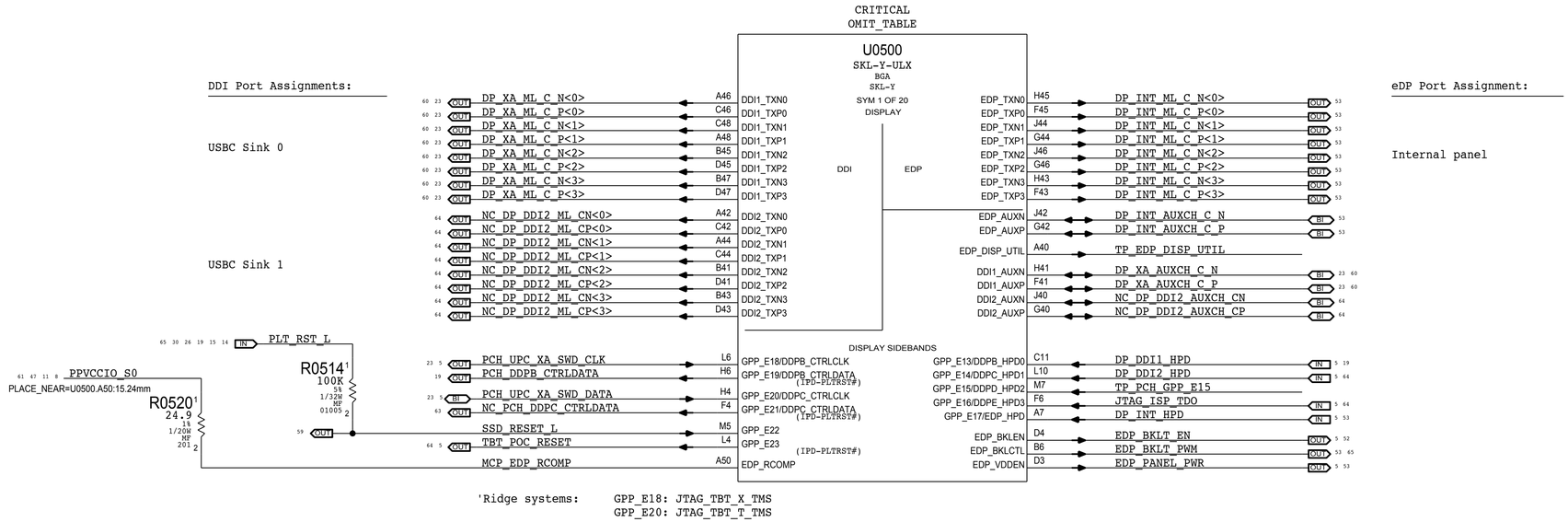
DRAWING NUMBER <SCH_NUM> SIZE D

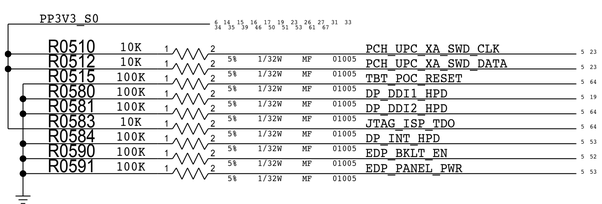
REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 4 OF 130

SHEET 4 OF 67





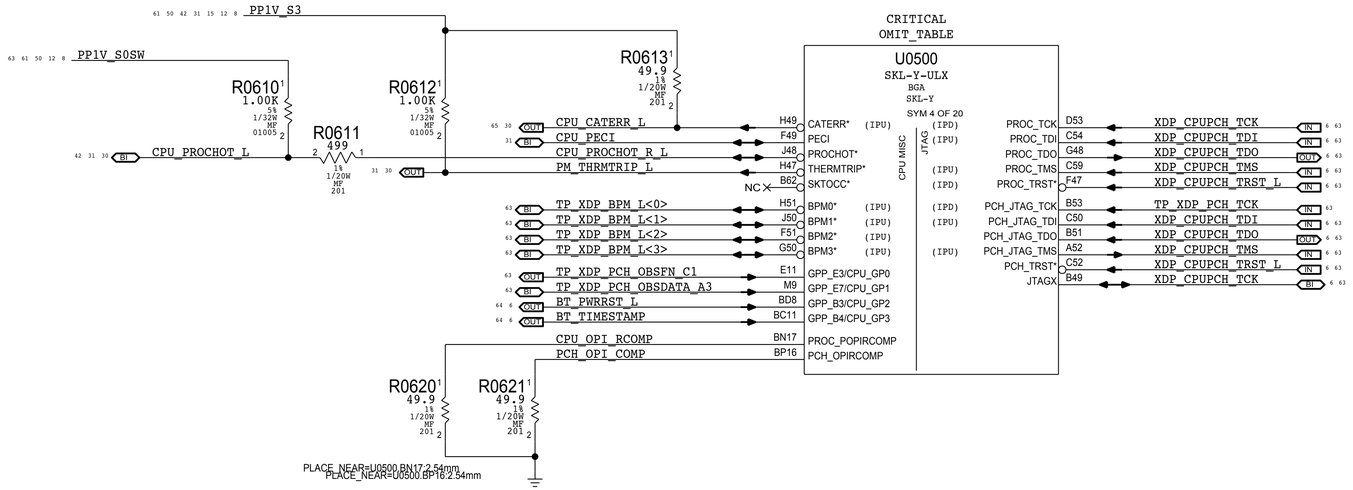
BOM_COST_GROUP=CPU & CHIPSET

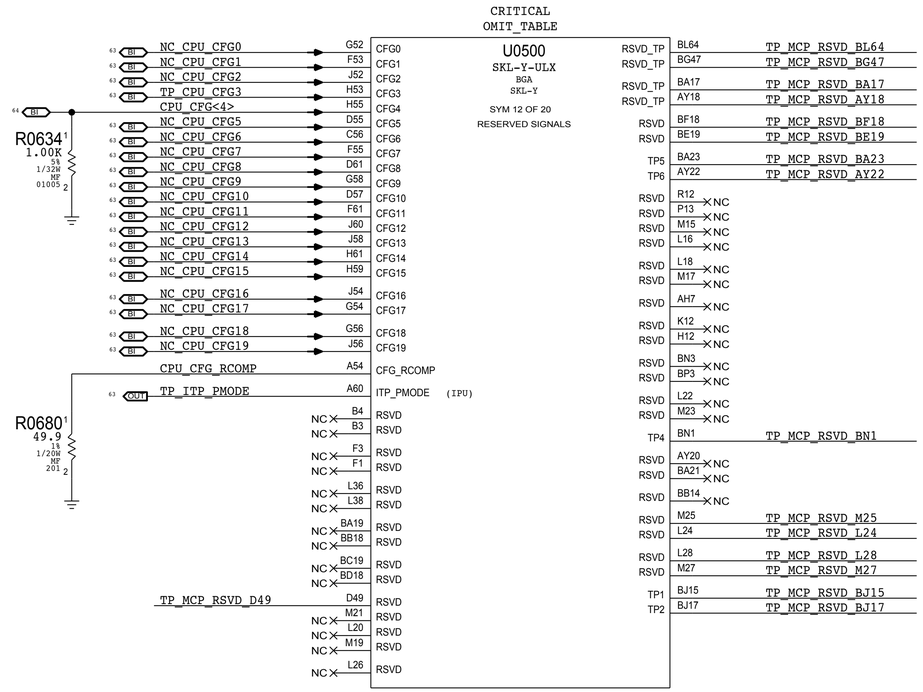
SYNC_MASTER=DEVMLB SYNC_DATE=05/11/2015

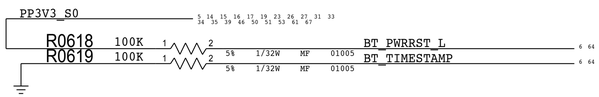
PAGE TITLE: CPU GFX

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 5 OF 130
SHEET: 5 OF 67







BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=DEVMLB SYNC_DATE=05/11/2015

PAGE TITLE: CPU Misc/JTAG/CFG/RSVD

Apple Inc.

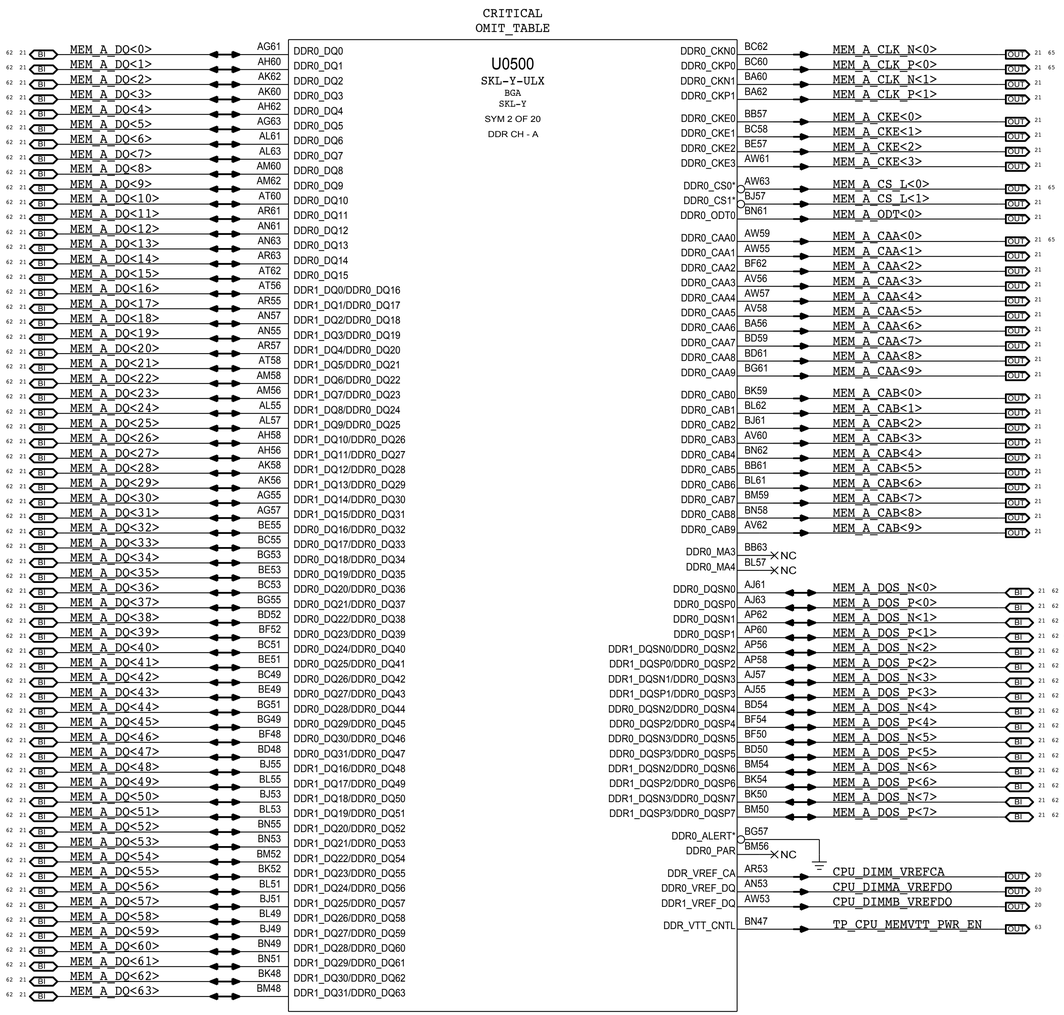
DRAWING NUMBER: <SCH_NUM> SIZE: D

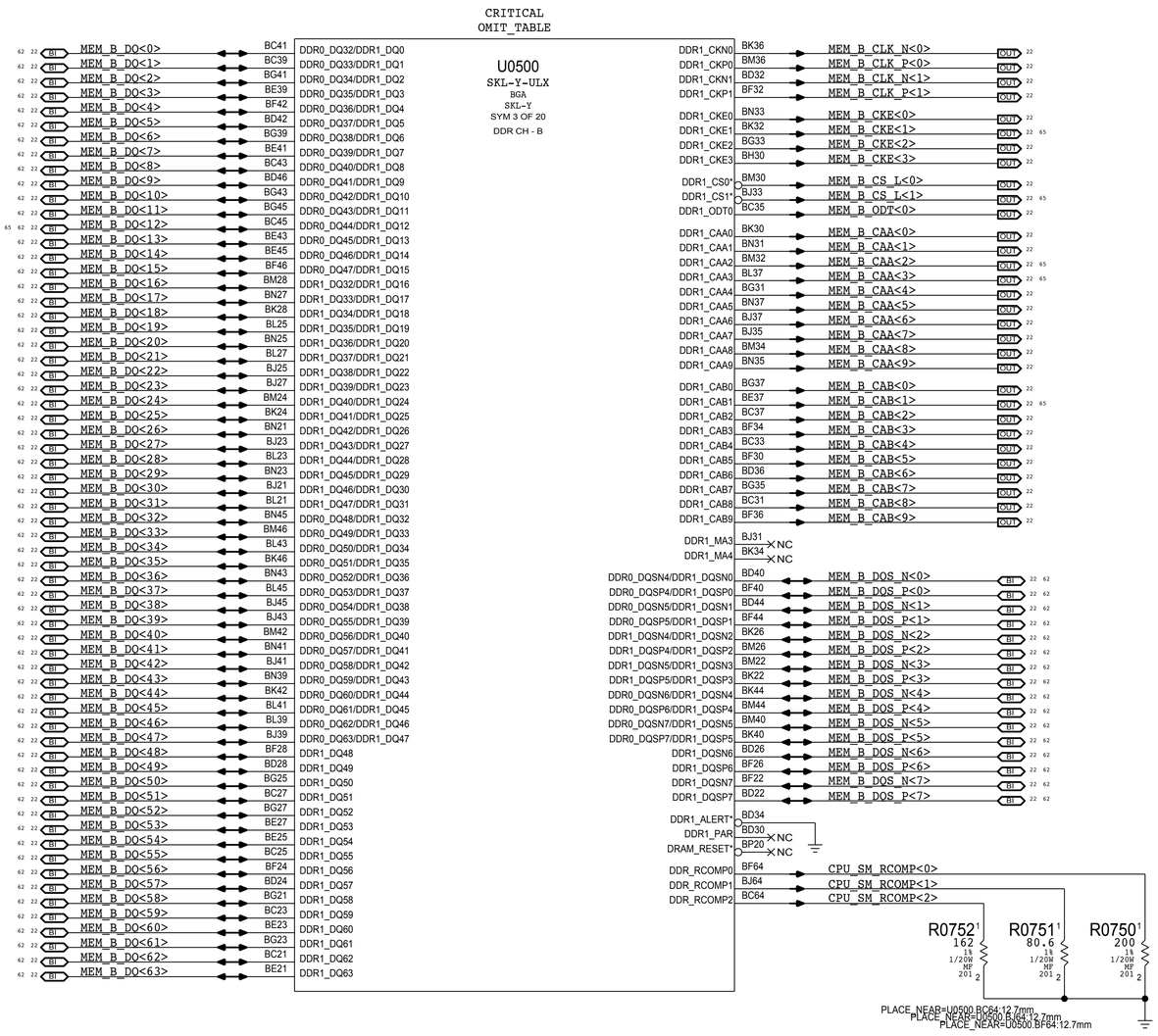
REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 6 OF 130

SHEET: 6 OF 67





BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=DEVMLB SYNC_DATE=04/14/2015

PAGE TITLE

CPU LPDDR3 Interface

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 7 OF 130

SHEET 7 OF 67

SKL-ULX current estimates from Skylake Processor EDS vol 1, doc #544924, v0.94
VCCIO breakdown per 4/20/15 email from Srini

NOTE: Aliases not used on CPU supply outputs
to avoid any extraneous connections.

CRITICAL
OMIT_TABLE

U0500
SKL-Y-ULX
BGA
SKL-Y
SYM 14 OF 20
CPU POWER 2 OF 4

34 12 8 61 44 PPVCORE_S0_GT
24A Max

AA53	VCCGT	VCCGT	AC53	PPVCORE_S0_GT	8 12 34 44 61
AB62	VCCGT	VCCGT	AC63		
AC47	VCCGT	VCCGT	AD62		
AC55	VCCGT	VCCGT	AE59		
AD54	VCCGT	VCCGT	AF46		
AD64	VCCGT	VCCGT	AG53		
AE61	VCCGT	VCCGT	AK47		
AF47	VCCGT	VCCGT	AN44		
AJ53	VCCGT	VCCGT	AN51		
AK49	VCCGT	VCCGT	AT49		
AN46	VCCGT	VCCGT	N48		
AT43	VCCGT	VCCGT	T44		
AT50	VCCGT	VCCGT	T51		
N50	VCCGT	VCCGT	U59		
T46	VCCGT	VCCGT	V58		
T54	VCCGT	VCCGT	W55		
U61	VCCGT	VCCGT	Y43		
V60	VCCGT	VCCGT	Y50		
W57	VCCGT	VCCGT	Y60		
Y44	VCCGT	VCCGT	AB56		
Y51	VCCGT	VCCGT	AC43		
Y62	VCCGT	VCCGT	AC50		
AB54	VCCGT	VCCGT	AC59		
AB64	VCCGT	VCCGT	AD58		
AC49	VCCGT	VCCGT	AE55		
AC57	VCCGT	VCCGT	AF43		
AD56	VCCGT	VCCGT	AF50		
AE53	VCCGT	VCCGT	AK44		
AE63	VCCGT	VCCGT	AK51		
AF49	VCCGT	VCCGT	AN49		
AK43	VCCGT	VCCGT	AT46		
AK50	VCCGT	VCCGT	N44		
AN47	VCCGT	VCCGT	R53		
AT44	VCCGT	VCCGT	T49		
AT51	VCCGT	VCCGT	U55		
R51	VCCGT	VCCGT	V54		
T47	VCCGT	VCCGT	V64		
U53	VCCGT	VCCGT	W61		
U63	VCCGT	VCCGT	Y47		
V62	VCCGT	VCCGT	Y56		
W59	VCCGT	VCCGT	AN50		
Y46	VCCGT	VCCGT	AT47		
Y54	VCCGT	VCCGT	N46		
Y64	VCCGT	VCCGT	T43		
AB58	VCCGT	VCCGT	T50		
AC44	VCCGT	VCCGT	U57		
AC51	VCCGT	VCCGT	V56		
AC61	VCCGT	VCCGT	W53		
AD60	VCCGT	VCCGT	W63		
AE57	VCCGT	VCCGT	Y49		
AF44	VCCGT	VCCGT	Y58		
AF51	VCCGT	VCCGT	AN43		
AK46	VCCGT				
AB60	VCCGT	VCCGT_SENSE	N52	CPU_VCCGTSENSE_P	OUT 42
AC46	VCCGT	VSSGT_SENSE	P52	CPU_VCCGTSENSE_N	OUT 42

PLACE_NEAR=U0500.N52:50.8mm
R0830 1 100 5% 1/32W MF 01005 2

PLACE_NEAR=U0500.P52:50.8mm
R0831 1 100 5% 1/32W MF 01005 2

CRITICAL
OMIT_TABLE

U0500
SKL-Y-ULX
BGA
SKL-Y
SYM 16 OF 20
CPU POWER 4 OF 4

61 43 11 PPVCCSA_S0
3.78A Max

AA29	VCCSA	VCCG0	AA35	PPVCCG0_S0_CPU	11
AF30	VCCSA	VCCG0	R38	MIN_LINE_WIDTH=0.2000	
AN29	VCCSA	VCCG0	Y35	MIN_NECK_WIDTH=0.2000	
L30	VCCSA	VCCG0	AA38	VOLTAGE=1.5V	
T30	VCCSA	VCCG0	T35		
AC29	VCCSA	VCCG0	Y38		
AH29	VCCSA	VCCG0	AC35		
AN30	VCCSA	VCCG0	T38		
M31	VCCSA	VCCG0	AC38		
V29	VCCSA	VCCG0	V35		
AC30	VCCSA	VCCG0	R35		
AK29	VCCSA	VCCG0	V38		
AR29	VCCSA				
N30	VCCSA	VCCG1	AF35	PPVCCG1_S0_CPU	11
Y29	VCCSA	VCCG1	AK38	MIN_LINE_WIDTH=0.2000	
AE29	VCCSA	VCCG1	AR35	MIN_NECK_WIDTH=0.2000	
AK30	VCCSA	VCCG1	AF38	VOLTAGE=1.5V	
R29	VCCSA	VCCG1	AL35		
Y30	VCCSA	VCCG1	AR38		
AF29	VCCSA	VCCG1	AH35		
AL29	VCCSA	VCCG1	AL38		
T29	VCCSA	VCCG1	AH38		
AT29	VCCSA_DDR	VCCG1	AN35		
AT30	VCCSA_DDR	VCCG1	AK35		
M29	VCCSA_SENSE	VCCG1	AN38		
N28	VSSSA_SENSE				

PLACE_NEAR=U0500.N30:50.8mm
R0860 1 100 5% 1/32W MF 01005 2

VCCSA & VCCSA_DDR must
be isolated from VR
output to BGA pads

61 43 11 PPVCCSA_DDR_S0
320mA Max

42 OUT CPU_VCCSASENSE_P
42 OUT CPU_VCCSASENSE_N

PLACE_NEAR=U0500.R30:50.8mm
R0861 1 100 5% 1/32W MF 01005 2

24A Max
61 43 34 11 8 PPVCORE_S0_CPU
TP_MCP_DC_A64

CRITICAL
OMIT_TABLE

U0500
SKL-Y-ULX
BGA
SKL-Y
SYM 13 OF 20
CPU POWER 1 OF 4

A64	VCC	VCC	M58	PPVCORE_S0_CPU	8 11 34 43 61
AE32	VCC	VCC	N34		
AE40	VCC	VCC	N54		
AH41	VCC	VCC	N63		
AN32	VCC	VCC	P64		
AT33	VCC	VCC	R61		
AT41	VCC	VCC	V41		
J64	VCC	VCC	AC41		
L48	VCC	VCC	AE38		
M33	VCC	VCC	AH32		
M43	VCC	VCC	AL41		
M53	VCC	VCC	AT32		
M64	VCC	VCC	AT40		
N40	VCC	VCC	H63		
N59	VCC	VCC	L46		
P60	VCC	VCC	L63		
R57	VCC	VCC	M41		
T41	VCC	VCC	M51		
AA32	VCC	VCC	M62		
AE33	VCC	VCC	N38		
AE41	VCC	VCC	N57		
AK32	VCC	VCC	P58		
AN41	VCC	VCC	R41		
AT35	VCC	VCC	T32		
B64	VCC	VCC	Y41		
L40	VCC	VCC	AC32		
L50	VCC	VCC	AE36		
M35	VCC	VCC	AF41		
M45	VCC	VCC	AL32		
M56	VCC	VCC	AR41		
N32	VCC	VCC	AT38		
N42	VCC	VCC	F64		
N61	VCC	VCC	L44		
P62	VCC	VCC	L54		
R59	VCC	VCC	M39		
V32	VCC	VCC	M49		
AA41	VCC	VCC	M60		
AE35	VCC	VCC	N36		
AF32	VCC	VCC	N55		
AK41	VCC	VCC_SENSE	L34	CPU_VCCSENSE_P	OUT 42
AR32	VCC	VSS_SENSE	L32	CPU_VCCSENSE_N	OUT 42
AT36	VCC	VIDALERT	B58	CPU_VIDALERT_R_L	
D64	VCC	VIDSCK	A56	CPU_VIDSCLK_R	
L42	VCC	VIDSOUT	A58	CPU_VIDSOUT_R	
L52	VCC	VCCSTG	AA26	PP1V_S0SW	6 8 61 12 50
M37	VCC	VCCSTG	AC26		
M47	VCC				
R63	VCC				
P56	VCC				
R32	VCC				
Y32	VCC				

TP_MCP_DC_B64

PLACE_NEAR=U0500.L34:50.8mm
R0820 1 100 5% 1/32W MF 01005 2

PLACE_NEAR=U0500.L32:50.8mm
R0821 1 100 5% 1/32W MF 01005 2

PP1V_S3 6 8 12 15 31 42 50 61

R0800 1 56 1% 1/20W MF 201 2
R0802 1 100 1% 1/20W MF 201 2

R0810 1 220 1% 1/20W MF 201 2 CPU_VIDALERT_L IN 42
R0811 1 0 5% 1/20W MF 0201 2 CPU_VIDSCLK OUT 42
R0812 1 0 5% 1/20W MF 0201 2 CPU_VIDSOUT BI 42

R0800.2: PLACE_NEAR=U0500.B58:12.7mm
R0802.2: PLACE_NEAR=U0500.A58:12.7mm
R0811.1: PLACE_NEAR=U0500.A56:12.7mm

CRITICAL
OMIT_TABLE

U0500
SKL-Y-ULX
BGA
SKL-Y
SYM 15 OF 20
CPU POWER 3 OF 4

61 50 47 22 21 20 12 PP1V2_S3
2A Max

AH64	VDDQ	VCCIO	AC23	PPVCCIO_S0	5 8 11 47 61
BA27	VDDQ	VCCIO	AF24	1.185A Max	
BA37	VDDQ	VCCIO	AN26		
BA49	VDDQ	VCCIO	AC24		
BP32	VDDQ	VCCIO	AF26		
BP50	VDDQ	VCCIO	AR26		
AK64	VDDQ	VCCIO	AE23		
BA29	VDDQ	VCCIO	AH26		
BA41	VDDQ	VCCIO	AT26		
BA51	VDDQ	VCCIO	AE24		
BP34	VDDQ	VCCIO	AK26	VCCIO & VCCIO_DDR must	
BP56	VDDQ	VCCIO	AE26	be isolated from local	
AT64	VDDQ	VCCIO	AL26	plane to BGA pads	
BA31	VDDQ	VCCIO_DDR	AV26	PPVCCIO_S0	5 8 11 47 61
BA43	VDDQ	VCCIO_DDR	AV36	1.75A Max	
BN64	VDDQ	VCCIO_DDR	AV46		
BP40	VDDQ	VCCIO_DDR	AW31		
BP58	VDDQ	VCCIO_DDR	AW41		
AV64	VDDQ	VCCIO_DDR	AW51		
BA33	VDDQ	VCCIO_DDR	AV28		
BA45	VDDQ	VCCIO_DDR	AV38		
BP24	VDDQ	VCCIO_DDR	AV48		
BP42	VDDQ	VCCIO_DDR	AW33		
BP64	VDDQ	VCCIO_DDR	AW43		
BA25	VDDQ	VCCIO_DDR	AV30		
BA35	VDDQ	VCCIO_DDR	AV40		
BA47	VDDQ	VCCIO_DDR	AV50		
BP26	VDDQ	VCCIO_DDR	AW35		
BP48	VDDQ	VCCIO_DDR	AW45		
BA39	VDDQC	VCCIO_DDR	AV32		
V26	VCCST	VCCIO_DDR	AV42		
Y26	VCCST	VCCIO_DDR	AW27		
R26	VCCSTG	VCCIO_DDR	AW37		
T26	VCCSTG	VCCIO_DDR	AW47		
AE27	VCCPLL_OC	VCCIO_DDR	AV34		
AF27	VCCPLL_OC	VCCIO_DDR	AW29		
R27	VCCPLL	VCCIO_DDR	AW39		
T27	VCCPLL	VCCIO_DDR	AW49		
		VCCIO_SENSE	AT24	CPU_VCCIOSENSE_P	OUT 47
		VSSIO_SENSE	AR24	CPU_VCCIOSENSE_N	OUT 47

TP_MCP_DC_BN64
TP_MCP_DC_BP64

VDDQC must implement
1nH trace filter

BYPASS=U0500.BA39::0.59mm

XW0850 SM 1 2
PP1V2_S0_CPU_VDDQC
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.2000
VOLTAGE=1.2V

C0850 1 0.1UF 10% 10V X5R-CERM 0201 2
61 50 42 15 12 8 6 31
61 50 12 8 6 63
PP1V_S3
PP1V_S0SW
61 50 12 PP1V2_S0SW
61 50 42 31 15 12 8 6 PP1V_S3

PLACE_NEAR=U0500.AT26:50.8mm
R0840 1 100 5% 1/32W MF 01005 2

PLACE_NEAR=U0500.AN24:50.8mm
R0841 1 100 5% 1/32W MF 01005 2

BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=DEVMLB SYNC_DATE=05/11/2015

PAGE TITLE
CPU Power

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 8 OF 130
SHEET 8 OF 67

SPT-LP current estimates from Sunrise Point-LP PCH EDS vol 1, doc #545659, v1.2.
VCCAMPHYPLL_1P0 and VCCPRIM_1P0 / VCCPRIM_3P3 breakdowns from Srini email 4/13/15

NOTE: Aliases not used on CPU supply outputs
to avoid any extraneous connections.

CRITICAL
OMIT_TABLE

U0500
SKL-Y-ULX
BGA
SKL-Y
SYM 17 OF 20
PCH POWER

PP1V_SUS
370mA Max
AH18 VCCPRIM_1P0
AH19 VCCPRIM_1P0
AK18 VCCPRIM_1P0
AL18 VCCPRIM_1P0

PPVCORE_SUS_PCH
1.1A Max
AE18 VCCPRIM_CORE
AE19 VCCPRIM_CORE
AF18 VCCPRIM_CORE
AF19 VCCPRIM_CORE
AR16 VCCPRIM_CORE
AT16 VCCPRIM_CORE

BYPASS=U0500.AL2::5.32mm
PP1V_S5_PCH_DCPDSW
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.2000
VOLTAGE=1.0V
AL2 DCPDSW_1P0
AM1 DCPDSW_1P0

C0920 1.0UF 20% 6.3V X5R 0201-1
PP1V_SUS
22mA Max
V1 VCCMPHYAON_1P0
W2 VCCMPHYAON_1P0

PP1V_SUSSW_HSIO
Project specific (X260 TBD)
See EDS Table 10-5
T1 VCCMPHYGT_1P0
T15 VCCMPHYGT_1P0
T16 VCCMPHYGT_1P0
U2 VCCMPHYGT_1P0

PP1V_SUSSW_PCH_VCCAMPHYPLL
88mA Max
V15 VCCAMPHYPLL_1P0
V16 VCCAMPHYPLL_1P0

PP1V_SUS_PCH_VCCAPLL
26mA Max
AA18 VCCAPLL_1P0
AA19 VCCAPLL_1P0

PP1V_SUS
168mA Max
AH13 VCCPRIM_1P0
AH15 VCCPRIM_1P0

PP3V3_S5
71mA Max
AL15 VCCDSW_3P3
AM13 VCCDSW_3P3

PP3V3R1V8R1V5_S0_PCH_VCCHDA
68/36/33mA @ 3.3/1.8/1.5V Max
AT23 VCCHDA
AV22 VCCHDA

PP3V3_SUS
11/7mA @ 3.3/1.8V Max
AT15 VCCSPI
AV15 VCCSPI

PP1V_SUSSW_HSIO
0.565A Max
AA21 VCCSRAM_1P0
AA23 VCCSRAM_1P0
AK23 VCCSRAM_1P0
AL23 VCCSRAM_1P0
AN23 VCCSRAM_1P0
AR23 VCCSRAM_1P0

PP3V3_SUS
74mA Max
AH21 VCCPRIM_3P3
AK21 VCCPRIM_3P3

PP1V_SUS
55mA Max
AR21 VCCPRIM_1P0
AT21 VCCPRIM_1P0

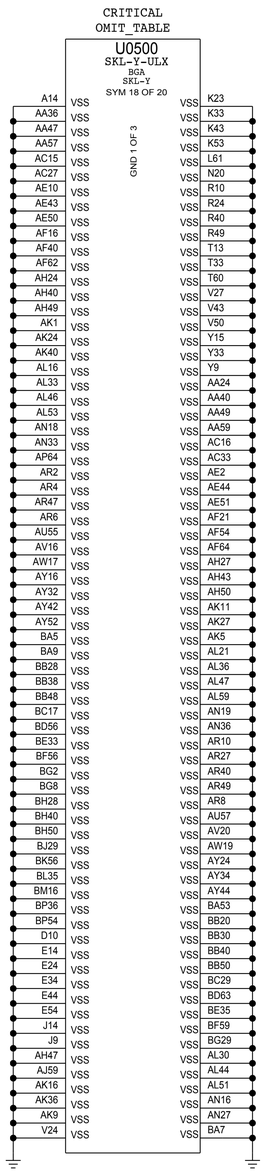
PP1V_SUSSW_HSIO
33mA Max
R15 VCCAPLLEBB_1P0
R16 VCCAPLLEBB_1P0

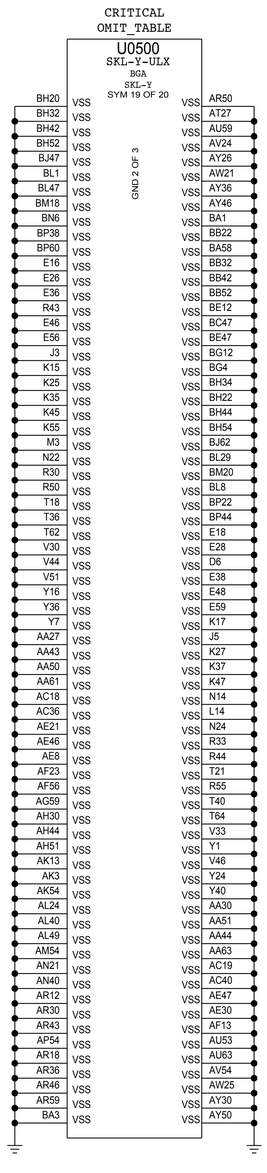
VCCPGPPA AT1 PP3V3_SUS
VCCPGPPA AU2 20/9mA @ 3.3/1.8V Max
VCCPGPPB AV1 PP3V3_SUS
VCCPGPPB AW2 4/2mA @ 3.3/1.8V Max
VCCPGPPC AH1 PP3V3_SUS
VCCPGPPC AJ2 6/3mA @ 3.3/1.8V Max
VCCPGPPD AF1 PP3V3_SUS
VCCPGPPD AG2 8/3mA @ 3.3/1.8V Max
VCCPGPPE AA2 PP3V3_SUS
VCCPGPPE AB1 6/2mA @ 3.3/1.8V Max
VCCPGPPF AN2 PP1V8_SUS
VCCPGPPF AP1 33/161mA @ 3.3/1.8V Max
VCCPGPPG AN15 PP3V3_SUS
VCCPGPPG AP13 41/56mA @ 3.3/1.8V Max
VCCPRIM_3P3 AC2 PP3V3_SUS
VCCPRIM_3P3 AD1 1mA Max
VCCPRIM_1P0 AA15 PP1V_SUS
VCCPRIM_1P0 AA16 6mA Max
VCCATS AE15 PP1V8_SUS
VCCATS AE16 6mA Max
VCCRTCPRIM_3P3 AK19 PP3V3_SUS
VCCRTCPRIM_3P3 AL19 <1mA Max
VCCRTC AR19
VCCRTC AT19 <1mA Max
DCPRTC AT18 PPVOUT_S0_PCH_DCPRTC
DCPRTC AV18 MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.2000 VOLTAGE=1.0V
VCCCLK1 V18 PP1V_SUS
VCCCLK1 Y18 35mA Max
VCCCLK2 V19 PP1V_SUS
VCCCLK2 Y19 29mA Max
VCCCLK3 V23 PP1V_SUS_PCH_VCCCLK3
VCCCLK3 Y23 24mA Max
VCCCLK4 V21 PP1V_SUS_PCH_VCCCLK4
VCCCLK4 Y21 33mA Max
VCCCLK5 R21 PP1V_SUS_PCH_VCCCLK5
VCCCLK5 R23 4mA Max
VCCCLK6 R19 PP1V_SUS
VCCCLK6 T19 10mA Max
GPP_B0/CORE_VID0 BA13 TP_PCH_CORE_VID<0>
GPP_B1/CORE_VID1 BB12 TP_PCH_CORE_VID<1>

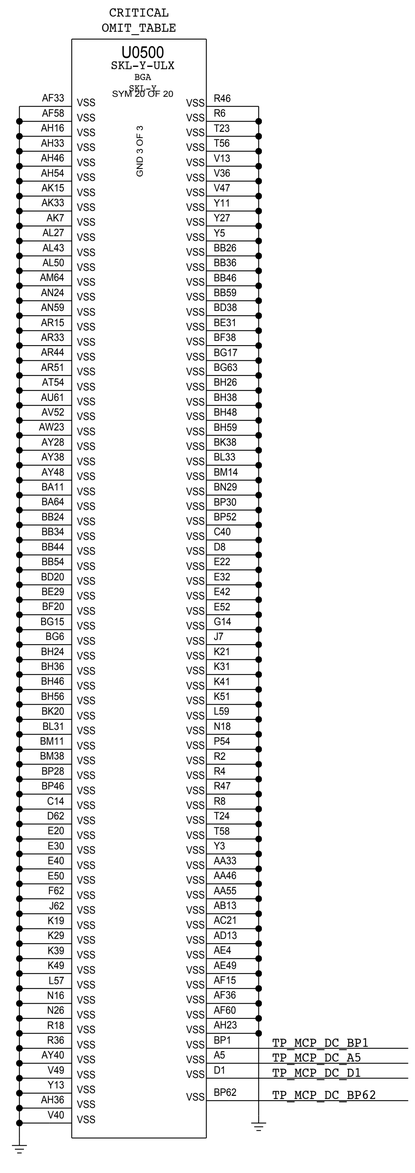
Must not exceed
3.2V max
PPVRTC_G3H
C0900 0.1UF 10% 10V X5R-CERM 0201
C0901 1.0UF 20% 6.3V X5R 0201-1
C0910 0.1UF 10% 10V X5R-CERM 0201
BYPASS=U0500.AR19::2.10mm
BYPASS=U0500.AT19::2.10mm
BYPASS=U0500.AT18::1.08mm

BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=DEVMLB SYNC_DATE=05/11/2015
PAGE TITLE
PCH Power
Apple Inc.
DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 9 OF 130
SHEET 9 OF 67







BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=DEVMLB SYNC_DATE=04/14/2015

PAGE TITLE

CPU & PCH Grounds

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 10 OF 130

SHEET 10 OF 67

All Intel recommendations from Intel doc #543016 Skylake U and Y Platform Design Guide Rev 1.3 unless stated otherwise
Intel's placeholders are no longer required per 4/20/15 email from Srini

CPU VCORE Decoupling

Intel recommendation (Table 52-2): 20x 0.1uF 0201 STUFF, 8x 10uF 0402, 6x 47uF 6.3V 0805 STUFF (2x NO STUFF)
Apple implementation : 20x 0.1uF 0201 STUFF (6x NO STUFF), 16x 20uF 0402, 3x 270uF 2V B2

61 43 34 9 PPVCORE_S0_CPU

C1100 0.1UF 10% 6.3V CERM-X5R 0201
C1101 0.1UF 10% 6.3V CERM-X5R 0201
C1102 0.1UF 10% 6.3V CERM-X5R 0201
C1103 0.1UF 10% 6.3V CERM-X5R 0201
C1104 0.1UF 10% 6.3V CERM-X5R 0201
C1105 0.1UF 10% 6.3V CERM-X5R 0201
C1106 0.1UF 10% 6.3V CERM-X5R 0201
C1107 0.1UF 10% 6.3V CERM-X5R 0201
C1108 0.1UF 10% 6.3V CERM-X5R 0201
C1109 0.1UF 10% 6.3V CERM-X5R 0201
C110A 0.1UF 10% 6.3V CERM-X5R 0201
C110B 0.1UF 10% 6.3V CERM-X5R 0201
C110C 0.1UF 10% 6.3V CERM-X5R 0201
C110D 0.1UF 10% 6.3V CERM-X5R 0201
C110E 0.1UF 10% 6.3V CERM-X5R 0201
C110F 0.1UF 10% 6.3V CERM-X5R 0201
C1110 0.1UF 10% 6.3V CERM-X5R 0201
C1111 0.1UF 10% 6.3V CERM-X5R 0201
C1112 0.1UF 10% 6.3V CERM-X5R 0201
C1113 0.1UF 10% 6.3V CERM-X5R 0201
NO STUFF C1114 0.1UF 10% 6.3V CERM-X5R 0201
NO STUFF C1115 0.1UF 10% 6.3V CERM-X5R 0201

NO STUFF C1116 0.1UF 10% 6.3V CERM-X5R 0201
NO STUFF C1117 0.1UF 10% 6.3V CERM-X5R 0201
NO STUFF C1118 0.1UF 10% 6.3V CERM-X5R 0201
NO STUFF C1119 0.1UF 10% 6.3V CERM-X5R 0201
C1132 12PF 5% 25V NPO-COG 0201
C1133 12PF 5% 25V NPO-COG 0201
CRITICAL C1120 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C1121 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C1122 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C1123 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C1124 20UF 20% 2.5V X6S-CERM 0402
NO STUFF C1125 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C1126 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C1127 20UF 20% 2.5V X6S-CERM 0402
NO STUFF C1128 20UF 20% 2.5V X6S-CERM 0402
NO STUFF C1129 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C112A 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C112B 20UF 20% 2.5V X6S-CERM 0402

CRITICAL C112C 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C112D 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C112E 20UF 20% 2.5V X6S-CERM 0402
NO STUFF C112F 20UF 20% 2.5V X6S-CERM 0402
OMIT_TABLE C1130 220UF 20% 2.0V POLY-TANT D15T-D1L-COMBO
OMIT_TABLE C1131 220UF 20% 2.0V POLY-TANT D15T-D1L-COMBO

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
128S00041	2	CAP,AL,POLY,220UF,20%,2V	C1130,C1131	CRITICAL	

CPU VCORE G0 Decoupling

Intel recommendation (Table 52-2): 12x 0.1uF 0201
Apple implementation : 12x 0.1uF 0201

9 PPVCCG0_S0_CPU

C1140 0.1UF 10% 6.3V CERM-X5R 0201
C1141 0.1UF 10% 6.3V CERM-X5R 0201
C1142 0.1UF 10% 6.3V CERM-X5R 0201
C1143 0.1UF 10% 6.3V CERM-X5R 0201
C1144 0.1UF 10% 6.3V CERM-X5R 0201
C1145 0.1UF 10% 6.3V CERM-X5R 0201
C1146 0.1UF 10% 6.3V CERM-X5R 0201
C1147 0.1UF 10% 6.3V CERM-X5R 0201
C1148 0.1UF 10% 6.3V CERM-X5R 0201
C1149 0.1UF 10% 6.3V CERM-X5R 0201
C114A 0.1UF 10% 6.3V CERM-X5R 0201
C114B 0.1UF 10% 6.3V CERM-X5R 0201

CPU VCORE G1 Decoupling

Intel recommendation (Table 52-2): 12x 0.1uF 0201
Apple implementation : 12x 0.1uF 0201

9 PPVCCG1_S0_CPU

C1150 0.1UF 10% 6.3V CERM-X5R 0201
C1151 0.1UF 10% 6.3V CERM-X5R 0201
C1152 0.1UF 10% 6.3V CERM-X5R 0201
C1153 0.1UF 10% 6.3V CERM-X5R 0201
C1154 0.1UF 10% 6.3V CERM-X5R 0201
C1155 0.1UF 10% 6.3V CERM-X5R 0201
C1156 0.1UF 10% 6.3V CERM-X5R 0201
C1157 0.1UF 10% 6.3V CERM-X5R 0201
C1158 0.1UF 10% 6.3V CERM-X5R 0201
C1159 0.1UF 10% 6.3V CERM-X5R 0201
C115A 0.1UF 10% 6.3V CERM-X5R 0201
C115B 0.1UF 10% 6.3V CERM-X5R 0201

CPU VCCIO Decoupling

Intel recommendation (Table 52-2): 13X 0.1UF 0201 STUFF (10x NO STUFF), 1x 1uF 0402, 1x 22uF 0805
Apple implementation : 13x 0.1uF 0201 STUFF (10x NO STUFF), 1x 1uF 0201, 1x 20uF 0402

61 47 8 5 PPVCCIO_S0

C1160 0.1UF 10% 6.3V CERM-X5R 0201
C1161 0.1UF 10% 6.3V CERM-X5R 0201
C1162 0.1UF 10% 6.3V CERM-X5R 0201
C1163 0.1UF 10% 6.3V CERM-X5R 0201
C1164 0.1UF 10% 6.3V CERM-X5R 0201
C1165 0.1UF 10% 6.3V CERM-X5R 0201
C1166 0.1UF 10% 6.3V CERM-X5R 0201
C1167 0.1UF 10% 6.3V CERM-X5R 0201
C1168 0.1UF 10% 6.3V CERM-X5R 0201
C1169 0.1UF 10% 6.3V CERM-X5R 0201
C116A 0.1UF 10% 6.3V CERM-X5R 0201
C116B 0.1UF 10% 6.3V CERM-X5R 0201
C116C 0.1UF 10% 6.3V CERM-X5R 0201
C1177 1.0UF 20% 6.3V X5R 0201-1
CRITICAL C1178 20UF 20% 2.5V X6S-CERM 0402

CPU VCCSA Decoupling

Intel recommendation (Table 52-2): 1x 1uF 0201, 4x 22uF 0603
Apple implementation : 1x 1uF 0201, 5x 0.1uF NO STUFF, 5x 20uF 0402, 1x 270uF 2V B2

61 43 8 PPVCCSA_S0

NO STUFF C1180 0.1UF 10% 6.3V CERM-X5R 0201
NO STUFF C1181 0.1UF 10% 6.3V CERM-X5R 0201
NO STUFF C1182 0.1UF 10% 6.3V CERM-X5R 0201
NO STUFF C1183 0.1UF 10% 6.3V CERM-X5R 0201
NO STUFF C1184 0.1UF 10% 6.3V CERM-X5R 0201
C118A 1.0UF 20% 6.3V X5R 0201-1
NO STUFF C118B 10UF 20% 4V X6S 0402
CRITICAL C118C 10UF 20% 4V X6S 0402
CRITICAL C118D 10UF 20% 4V X6S 0402
NO STUFF C118E 10UF 20% 4V X6S 0402
CRITICAL C118F 10UF 20% 4V X6S 0402
CRITICAL C1190 120UF 20% 2.5V TANT-POLY CASE-B2-SM

CPU VCCSA DDR Decoupling

Intel recommendation (Table 52-2): 1x 0.1uF 0201 STUFF, 1x 22uF 0603
Apple implementation : 1x 0.1uF 0201 STUFF, 1x 20uF 0402

61 43 8 PPVCCSA_DDR_S0

C1195 0.1UF 10% 6.3V CERM-X5R 0201
CRITICAL C1197 10UF 20% 4V X6S 0402

BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=DEVMLB SYNC_DATE=04/14/2015
PAGE TITLE: CPU Decoupling 1
Apple Inc.
DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 11 OF 130
SHEET: 11 OF 67

All Intel recommendations from Intel doc #543016 Skylake U and Y Platform Design Guide Rev 1.3 unless stated otherwise
Intel's placeholders are no longer required per 4/20/15 email from Srini

CPU GT Decoupling

Intel recommendation (Table 52-2): 12x 0.1uF 0201 STUFF, 2x 1uF 0402, 2x 10uF 0402 NO STUFF, 9x 47uF 6.3V 0805
Apple implementation : 12x 0.1uF 0201 STUFF (20x NO STUFF), 2x 1uF 0201, 16x 20uF 0402, 2x 270uF 2V B2

61 44 34 8 PPVCORE_S0_GT

C1200 0.1UF 10% 6.3V CERM-X5R 0201	C1201 0.1UF 10% 6.3V CERM-X5R 0201	C1202 0.1UF 10% 6.3V CERM-X5R 0201	C1203 0.1UF 10% 6.3V CERM-X5R 0201	C1204 0.1UF 10% 6.3V CERM-X5R 0201	C1205 0.1UF 10% 6.3V CERM-X5R 0201	C1206 0.1UF 10% 6.3V CERM-X5R 0201	C1207 0.1UF 10% 6.3V CERM-X5R 0201	C1208 0.1UF 10% 6.3V CERM-X5R 0201	C1209 0.1UF 10% 6.3V CERM-X5R 0201	C1210 0.1UF 10% 6.3V CERM-X5R 0201	C1211 0.1UF 10% 6.3V CERM-X5R 0201	NO STUFF C1212 0.1UF 10% 6.3V CERM-X5R 0201	NO STUFF C1213 0.1UF 10% 6.3V CERM-X5R 0201	NO STUFF C1214 0.1UF 10% 6.3V CERM-X5R 0201	NO STUFF C1215 0.1UF 10% 6.3V CERM-X5R 0201	NO STUFF C1216 0.1UF 10% 6.3V CERM-X5R 0201	NO STUFF C1217 0.1UF 10% 6.3V CERM-X5R 0201	NO STUFF C1218 0.1UF 10% 6.3V CERM-X5R 0201	NO STUFF C1219 0.1UF 10% 6.3V CERM-X5R 0201	NO STUFF C1220 0.1UF 10% 6.3V CERM-X5R 0201	NO STUFF C1221 0.1UF 10% 6.3V CERM-X5R 0201
NO STUFF C1222 0.1UF 10% 6.3V CERM-X5R 0201	NO STUFF C1223 0.1UF 10% 6.3V CERM-X5R 0201	NO STUFF C1224 0.1UF 10% 6.3V CERM-X5R 0201	NO STUFF C1225 0.1UF 10% 6.3V CERM-X5R 0201	NO STUFF C1226 0.1UF 10% 6.3V CERM-X5R 0201	NO STUFF C1227 0.1UF 10% 6.3V CERM-X5R 0201	NO STUFF C1228 0.1UF 10% 6.3V CERM-X5R 0201	NO STUFF C1229 0.1UF 10% 6.3V CERM-X5R 0201	NO STUFF C1230 0.1UF 10% 6.3V CERM-X5R 0201	NO STUFF C1231 0.1UF 10% 6.3V CERM-X5R 0201												
C1252 1.0UF 20% 6.3V X5R 0201-1	C1253 1.0UF 20% 6.3V X5R 0201-1	NO STUFF C1254 20UF 20% 2.5V X6S-CERM 0402	CRITICAL C1255 20UF 20% 2.5V X6S-CERM 0402	CRITICAL C1256 20UF 20% 2.5V X6S-CERM 0402	CRITICAL C1257 20UF 20% 2.5V X6S-CERM 0402	CRITICAL C1258 20UF 20% 2.5V X6S-CERM 0402	CRITICAL C1259 20UF 20% 2.5V X6S-CERM 0402	CRITICAL C125A 20UF 20% 2.5V X6S-CERM 0402	CRITICAL C125B 20UF 20% 2.5V X6S-CERM 0402	CRITICAL C125C 20UF 20% 2.5V X6S-CERM 0402	CRITICAL C125D 20UF 20% 2.5V X6S-CERM 0402	CRITICAL C125E 20UF 20% 2.5V X6S-CERM 0402	NO STUFF C125F 20UF 20% 2.5V X6S-CERM 0402								
NO STUFF C1260 20UF 20% 2.5V X6S-CERM 0402	CRITICAL C1261 20UF 20% 2.5V X6S-CERM 0402	CRITICAL C1262 20UF 20% 2.5V X6S-CERM 0402	NO STUFF C1263 20UF 20% 2.5V X6S-CERM 0402	CRITICAL C1264 270UF 20% 2V TANT CASE-B2-SM	CRITICAL C1265 270UF 20% 2V TANT CASE-B2-SM																	

CPU VDDQ DECOUPLING

Intel recommendation (Table 52-2): 18x 0.1uF 0201
Apple implementation : 18x 0.1uF 0201

50 47 22 21 20 8 61 PP1V2_S3

C1270 0.1UF 10% 6.3V CERM-X5R 0201	C1271 0.1UF 10% 6.3V CERM-X5R 0201	C1272 0.1UF 10% 6.3V CERM-X5R 0201	C1273 0.1UF 10% 6.3V CERM-X5R 0201	C1274 0.1UF 10% 6.3V CERM-X5R 0201	C1275 0.1UF 10% 6.3V CERM-X5R 0201	C1276 0.1UF 10% 6.3V CERM-X5R 0201	C1277 0.1UF 10% 6.3V CERM-X5R 0201	C1278 0.1UF 10% 6.3V CERM-X5R 0201	C1279 0.1UF 10% 6.3V CERM-X5R 0201
C1280 0.1UF 10% 6.3V CERM-X5R 0201	C1281 0.1UF 10% 6.3V CERM-X5R 0201	C1282 0.1UF 10% 6.3V CERM-X5R 0201	C1283 0.1UF 10% 6.3V CERM-X5R 0201	C1284 0.1UF 10% 6.3V CERM-X5R 0201	C1285 0.1UF 10% 6.3V CERM-X5R 0201	C1286 0.1UF 10% 6.3V CERM-X5R 0201	C1287 0.1UF 10% 6.3V CERM-X5R 0201		

CPU VCCST BYPASS
(CPU 1.0V SUSTAIN PWR)
42 31 15 12 8 6 61 50 PP1V_S3

C1290 0.1UF 10% 6.3V X6S 0201
BYPASS=U0500.V26::2.38mm

CPU VCCSTG BYPASS
(CPU 1.0V SUSTAIN GATED PWR)
63 61 50 8 6 PP1V_S0SW

C1292 0.1UF 10% 6.3V X6S 0201
BYPASS=U0500.R26::4.20mm

CPU VCCPLL_OC BYPASS
(CPU 1.2V PLL PWR)
61 50 9 PP1V2_S0SW

C1294 0.1UF 10% 6.3V X6S 0201
BYPASS=U0500.AE27::2.07mm

CPU VCCPLL BYPASS
(CPU 1.0V DIGITAL PLL PWR)
42 31 15 12 8 6 61 50 PP1V_S3

C1296 0.1UF 10% 6.3V X6S 0201
BYPASS=U0500.R27::1.99mm

NOTE: Bypass calcs based on 0.1mm trace width with worst case stackup and 500pH added for power/ground via pair.

BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=DEVMLB SYNC_DATE=05/06/2015

PAGE TITLE: CPU Decoupling 2

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 12 OF 130
SHEET: 12 OF 67

PCH VCCDSW_3P3 BYPASS
(PCH 3.3V DSW PWR)
PP3V3_S5
C1300 0.1UF 10% 6.3V X6S 0201
BYPASS=U0500.AL15::1.96mm

PCH VCCSPI BYPASS
(PCH 3.3V/1.8V SPI PWR)
PP3V3_SUS
C1302 0.1UF 10% 6.3V X6S 0201
BYPASS=U0500.AT15::2.38mm

PCH VCCRTCPRIM BYPASS
(PCH 3.3V SUSPEND RTC PWR)
PP3V3_SUS
C1306 1.0UF 20% 6.3V X5R 0201-1
C1307 0.1UF 10% 6.3V X6S 0201
BYPASS=U0500.AK19::1.68mm
BYPASS=U0500.AK19::1.68mm

PCH VCCPGPPE BYPASS
(PCH 3.3V/1.8V GPIO GROUP E PWR)
PP3V3_SUS
C1318 0.1UF 10% 6.3V X6S 0201
BYPASS=U0500.AA2::0.84mm

PCH VCCATS BYPASS
(PCH 1.8V THERMAL PWR)
PP1V8_SUS
C1330 1.0UF 20% 6.3V X5R 0201-1
BYPASS=U0500.AE15::1.76mm

PCH VCCMPHYAON_1P0 BYPASS
(PCH 1.0V MPHY ALWAYS ON PWR)
PP1V_SUS
C1340 0.1UF 10% 6.3V X6S 0201
BYPASS=U0500.V1::1.68mm

PCH VCCAPLLEBB BYPASS
(PCH 1.0V APLL EBB PWR)
PP1V_SUSSW_HSIO
C1344 0.1UF 10% 6.3V X6S 0201
BYPASS=U0500.R15::1.54mm

PCH VCCAMPHYPLL_1P0 FILTER/BYPASS
(PCH 1.0V USB3/PCIE/SATA/MIPI PLL PWR)
PP1V_SUSSW
R1370 0 5% 1/16W MF-LF 402
PP1V_SUSSW_PCH_VCCAMPHYPLL
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
VOLTAGE=1.0V
NOSTUFF C1370 20UF 20% 6.3V CERM-X5R 0402
NOSTUFF C1371 20UF 20% 6.3V CERM-X5R 0402
NOSTUFF C1372 0.1UF 10% 6.3V X6S 0201
BYPASS=U0500.V15::12.82mm
BYPASS=U0500.V15::12.82mm
BYPASS=U0500.V15::3.91mm

PCH VCCCLK3 FILTER/BYPASS
(PCH 1.0V CLOCK 3 PWR)
PP1V_SUS
R1380 0 5% 1/16W MF-LF 402
PP1V_SUS_PCH_VCCCLK3
MIN_LINE_WIDTH=0.0950
MIN_NECK_WIDTH=0.0700
VOLTAGE=1.0V
NOSTUFF C1380 20UF 20% 6.3V CERM-X5R 0402
NOSTUFF C1381 20UF 20% 6.3V CERM-X5R 0402
BYPASS=U0500.V19::10.17mm
BYPASS=U0500.V19::10.17mm

PCH VCCCLK4 FILTER/BYPASS
(PCH 1.0V CLOCK 4 PWR)
PP1V_SUS
R1385 0 5% 1/16W MF-LF 402
PP1V_SUS_PCH_VCCCLK4
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
VOLTAGE=1.0V
NOSTUFF C1385 20UF 20% 6.3V CERM-X5R 0402
NOSTUFF C1386 20UF 20% 6.3V CERM-X5R 0402
BYPASS=U0500.V21::10.17mm
BYPASS=U0500.V21::10.17mm

PCH VCCCLK5 FILTER/BYPASS
(PCH 1.0V CLOCK 5 PWR)
PP1V_SUS
R1390 0 5% 1/16W MF-LF 402
PP1V_SUS_PCH_VCCCLK5
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
VOLTAGE=1.0V
NOSTUFF C1390 20UF 20% 6.3V CERM-X5R 0402
NOSTUFF C1391 20UF 20% 6.3V CERM-X5R 0402
C1392 0.1UF 10% 6.3V X6S 0201
BYPASS=U0500.R21::10.17mm
BYPASS=U0500.R21::10.17mm
BYPASS=U0500.R21::0.92mm

PCH VCCHDA FILTER/BYPASS
(PCH 3.3V/1.8V/1.5V HDA PWR)
PP1V5_S0
L1309 220-OHM-0.7A-0.28-OHM 0402-1
PP3V3R1V8R1V5_S0_PCH_VCCHDA
MIN_LINE_WIDTH=0.0950
MIN_NECK_WIDTH=0.0700
VOLTAGE=1.5V
C1309 0.1UF 10% 6.3V X6S 0201
BYPASS=U0500.AT23::1.23mm

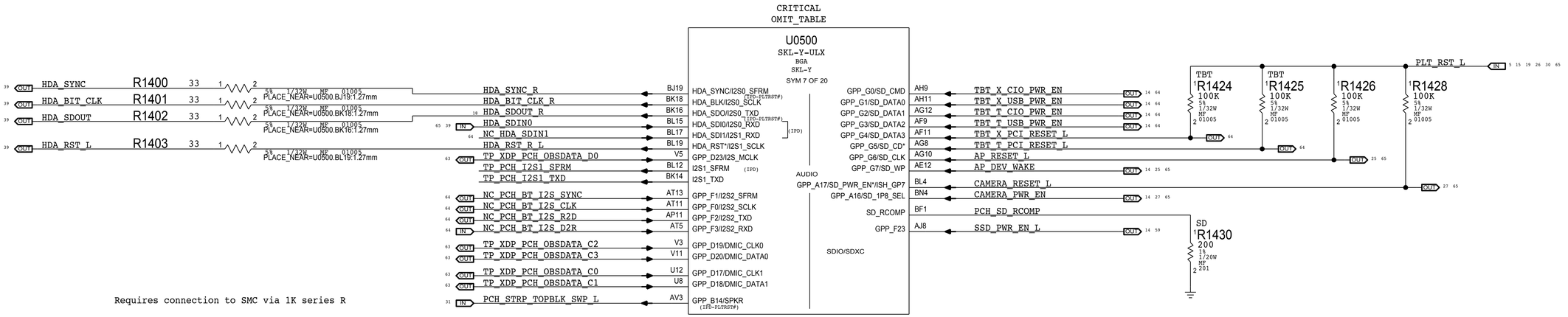
PCH VCCAPLL FILTER/BYPASS
(PCH 1.0V APLL PWR)
PP1V_SUS
L1395 220-OHM-0.7A-0.28-OHM 0402-1
PP1V_SUS_PCH_VCCAPLL
MIN_LINE_WIDTH=0.0950
MIN_NECK_WIDTH=0.0700
VOLTAGE=1.0V
C1395 0.1UF 10% 6.3V X6S 0201
BYPASS=U0500.AA18::1.23mm

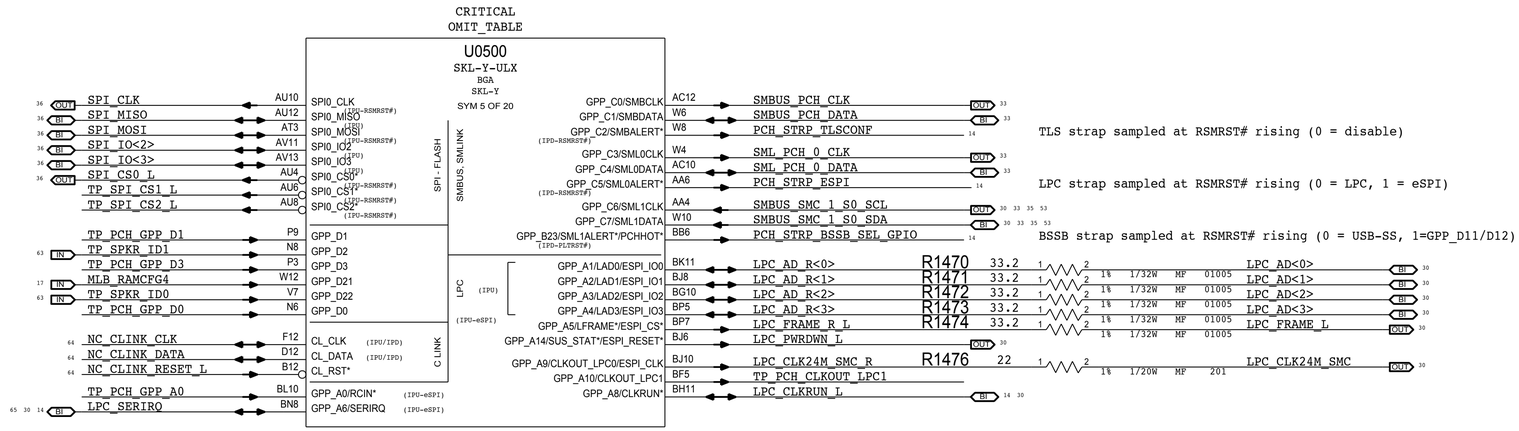
PCH VCCMPHYGT_1P0 BYPASS
(PCH 1.0V MPHY GATED PWR)
PP1V_SUSSW_HSIO
C1346 0.1UF 10% 6.3V X6S 0201
C1347 1.0UF 20% 6.3V X5R 0201-1
C1348 20UF 20% 6.3V CERM-X5R 0402
BYPASS=U0500.T15::3.07mm
BYPASS=U0500.T15::4.18mm
BYPASS=U0500.T15::4.18mm

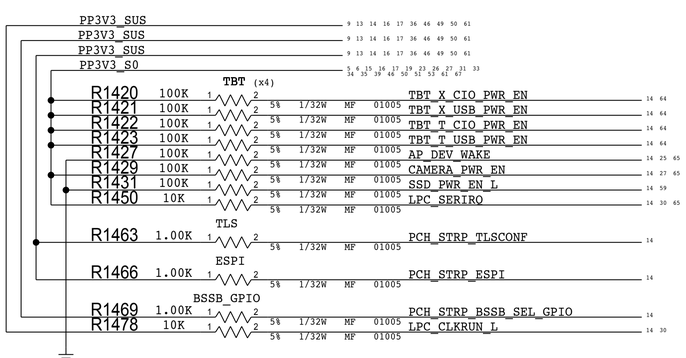
PCH VCCPRIM_1P0 BYPASS
(PCH 1.0V USB PWR)
PP1V_SUS
C1336 0.1UF 10% 6.3V X6S 0201
BYPASS=U0500.AH13::1.39mm

BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=DEVMLB SYNC_DATE=05/11/2015
PAGE TITLE
PCH Decoupling
Apple Inc.
DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 13 OF 130
SHEET 13 OF 67







BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=DEVMLB SYNC_DATE=05/11/2015

PAGE TITLE: PCH Audio/LPC/SPI/SMBus

Apple Inc.

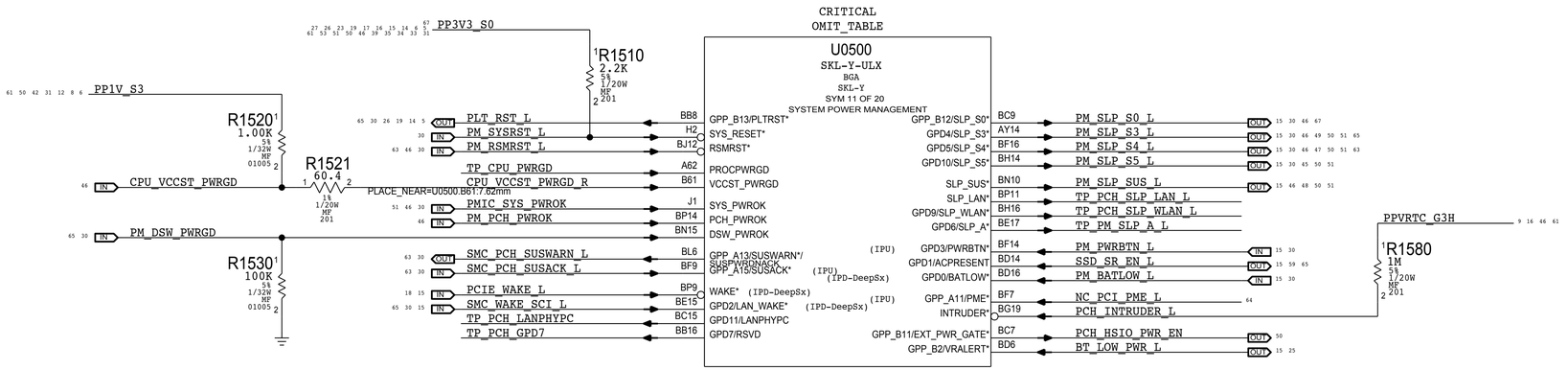
DRAWING NUMBER: <SCH_NUM> SIZE: D

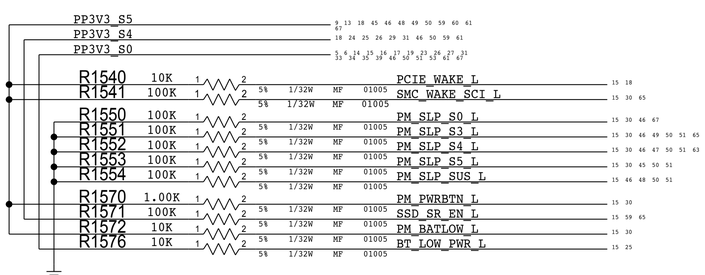
REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 14 OF 130

SHEET: 14 OF 67





BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=X260_ERIC SYNC_DATE=06/04/2015

PAGE TITLE

PCH Power Management

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 15 OF 130

SHEET 15 OF 67

PCIe Port Assignments:

SSD lane 0

SSD lane 1

SSD lane 2

SSD lane 3

Reserved: Thunderbolt A lane 0

Reserved: Thunderbolt A lane 1

Reserved: Thunderbolt B lane 0

Reserved: Thunderbolt B lane 1

Airport

Camera

CRITICAL
OMIT_TABLE

U0500
SKL-Y-ULX
BGA
SKL-Y
SYM 8 OF 20

PCIE_SSD_D2R_N<0>	C20	PCIE1_RXN/USB3_5_RXN	
PCIE_SSD_D2R_P<0>	A20	PCIE1_RXP/USB3_5_RXP	
PCIE_SSD_R2D_C_N<0>	G20	PCIE1_TXN/USB3_5_TXN	
PCIE_SSD_R2D_C_P<0>	J20	PCIE1_TXP/USB3_5_TXP	
PCIE_SSD_D2R_N<1>	B19	PCIE2_RXN/USB3_6_RXN	
PCIE_SSD_D2R_P<1>	D19	PCIE2_RXP/USB3_6_RXP	
PCIE_SSD_R2D_C_N<1>	F19	PCIE2_TXN/USB3_6_TXN	
PCIE_SSD_R2D_C_P<1>	H19	PCIE2_TXP/USB3_6_TXP	
NC_PCIE_SSD_D2RN<2>	C22	PCIE3_RXN	
NC_PCIE_SSD_D2RP<2>	A22	PCIE3_RXP	
NC_PCIE_SSD_R2D_CN<2>	G22	PCIE3_TXN	
NC_PCIE_SSD_R2D_CP<2>	J22	PCIE3_TXP	
NC_PCIE_SSD_D2RN<3>	B21	PCIE4_RXN	
NC_PCIE_SSD_D2RP<3>	D21	PCIE4_RXP	
NC_PCIE_SSD_R2D_CN<3>	F21	PCIE4_TXN	
NC_PCIE_SSD_R2D_CP<3>	H21	PCIE4_TXP	
PCIE_TEST_D2R_N	C24	PCIE5_RXN	
PCIE_TEST_D2R_P	A24	PCIE5_RXP	
PCIE_TEST_R2D_N	G24	PCIE5_TXN	
PCIE_TEST_R2D_P	J24	PCIE5_TXP	
TP_PCIE_TBT_A_D2RN<1>	B23	PCIE6_RXN	
TP_PCIE_TBT_A_D2RP<1>	D23	PCIE6_RXP	
TP_PCIE_TBT_A_R2D_CN<1>	F23	PCIE6_TXN	
TP_PCIE_TBT_A_R2D_CP<1>	H23	PCIE6_TXP	
TP_PCIE_TBT_B_D2RN<0>	C26	PCIE7_RXN/SATA0_RXN	
TP_PCIE_TBT_B_D2RP<0>	A26	PCIE7_RXP/SATA0_RXP	
TP_PCIE_TBT_B_R2D_CN<0>	G26	PCIE7_TXN/SATA0_TXN	
TP_PCIE_TBT_B_R2D_CP<0>	J26	PCIE7_TXP/SATA0_TXP	
TP_PCIE_TBT_B_D2RN<1>	B25	PCIE8_RXN/SATA1A_RXN	
TP_PCIE_TBT_B_D2RP<1>	D25	PCIE8_RXP/SATA1A_RXP	
TP_PCIE_TBT_B_R2D_CN<1>	F25	PCIE8_TXN/SATA1A_TXN	
TP_PCIE_TBT_B_R2D_CP<1>	H25	PCIE8_TXP/SATA1A_TXP	
PCIE_AP_D2R_N	C28	PCIE9_RXN	
PCIE_AP_D2R_P	A28	PCIE9_RXP	
PCIE_AP_R2D_C_N	G28	PCIE9_TXN	
PCIE_AP_R2D_C_P	J28	PCIE9_TXP	
PCIE_CAMERA_D2R_N	B27	PCIE10_RXN	
PCIE_CAMERA_D2R_P	D27	PCIE10_RXP	
PCIE_CAMERA_R2D_C_N	F27	PCIE10_TXN	
PCIE_CAMERA_R2D_C_P	H27	PCIE10_TXP	
PCH_PCIE_RCOMP_N	A9	PCIE_RCOMPN	
PCH_PCIE_RCOMP_P	B10	PCIE_RCOMPP	
TP_XDP_CPU_PRDY_L	D51	PROC_PRDY* (IPU)	
TP_XDP_CPU_PREQ_L	B55	PROC_PREQ* (IPU)	
SMC_RUNTIME_SCI_L	BF3	GPP_A7/PIRQA*	

SSIC / USB3

PCIE/USB3/SATA

USB2

USB3_1_RXN	C16	USB3_EXTA_D2R_N	
USB3_1_RXP	A16	USB3_EXTA_D2R_P	
USB3_1_TXN	G16	USB3_EXTA_R2D_C_N	
USB3_1_TXP	J16	USB3_EXTA_R2D_C_P	
USB3_2_RXN/SSIC_RXN	B15	NC_USB3_EXTB_D2RN	
USB3_2_RXP/SSIC_RXP	D15	NC_USB3_EXTB_D2RP	
USB3_2_TXN/SSIC_TXN	F15	NC_USB3_EXTB_R2D_CN	
USB3_2_TXP/SSIC_TXP	H15	NC_USB3_EXTB_R2D_CP	
USB3_3_RXN	C18	NC_USB3_EXTC_D2RN	
USB3_3_RXP	A18	NC_USB3_EXTC_D2RP	
USB3_3_TXN	G18	NC_USB3_EXTC_R2D_CN	
USB3_3_TXP	J18	NC_USB3_EXTC_R2D_CP	
USB3_4_RXN	B17	NC_USB3_EXTD_D2RN	
USB3_4_RXP	D17	NC_USB3_EXTD_D2RP	
USB3_4_TXN	F17	NC_USB3_EXTD_R2D_CN	
USB3_4_TXP	H17	NC_USB3_EXTD_R2D_CP	
USB2N_1	AJ6	USB_EXTA_N	
USB2P_1	AJ4	USB_EXTA_P	
USB2N_5	AH5	NC_USB_EXTDN	
USB2P_5	AH3	NC_USB_EXTDP	
USB2N_7	AF5	TP_USB_7N	
USB2P_7	AF3	TP_USB_7P	
USB2N_3	AL6	NC_USB_EXTCN	
USB2P_3	AL4	NC_USB_EXTCP	
USB2N_9	AG6	USB_TEST_N	
USB2P_9	AG4	USB_TEST_P	
USB2N_2	AM3	NC_USB_EXTBN	
USB2P_2	AM5	NC_USB_EXTBP	
(IPD) USB2_COMP	N2	PCH_USB2_COMP	
(IPU) USB2_ID	AF7		
USB2_VBUSSENSE	AE6	USB2_VBUSSENSE	

USB3 Port Assignments:

Ext A (SS, DCI)

Ext B (SS)

Ext C (SS)

Ext D (SS)

USB Port Assignments:

Ext A (LS/FS/HS)

Ext D (LS/FS/HS)

Unused

Ext C (LS/FS/HS)

Unused

Ext B (LS/FS/HS)

Grounded per SKL MOW 2015WW10

GPP_E9/USB2_OC0*	N12	XDP_USB_EXTA_OC_L	
GPP_E10/USB2_OC1*	M11	USB_EXTB_OC_L	
GPP_E11/USB2_OC2*	F8	XDP_USB_EXTC_OC_L	
(IPD-RSMRST#) GPP_E12/USB2_OC3*	B8	XDP_USB_EXTD_OC_L	
GPP_E4/DEVSLP0	F10	XDP_JTAG_ISP_TCK	
GPP_E5/DEVSLP1	H10	XDP_JTAG_ISP_TDI	
GPP_E6/DEVSLP2	L8	TP_XDP_PCH_OBSDATA_A2	
GPP_E0/SATAXPCIE0/SATAGP0	G11	TP_XDP_PCH_OBSDATA_D1	
GPP_E1/SATAXPCIE1/SATAGP1	J11	TP_XDP_PCH_OBSDATA_D2	
GPP_E2/SATAXPCIE2/SATAGP2	N10	TP_XDP_PCH_OBSDATA_D3	
GPP_E8/SATALED*	H8	TP_XDP_PCH_OBSDATA_B0	

R1620 1.00K 5% 1/32W MF 01005

PLACE_NEAR=U0500.N2:2.54mm
R1622 113 1% 1/20W MF 201

R1610 100 1% 1/20W MF 201
PLACE_NEAR=U0500.B10:2.54mm

CRITICAL
OMIT_TABLE

U0500
SKL-Y-ULX
BGA
SKL-Y
SYM 10 OF 20
CLOCK SIGNALS

PCIE_CLK100M_SSD_N	H35	CLKOUT_PCIE_N1	
PCIE_CLK100M_SSD_P	F35	CLKOUT_PCIE_P1	
TBT_X_CLKREQ_L	AV9	GPP_B6/SRCCLKREQ1*	
PCIE_CLK100M_TEST_N	J36	CLKOUT_PCIE_N2	
PCIE_CLK100M_TEST_P	G36	CLKOUT_PCIE_P2	
TEST_CLKREQ_L	BD10	GPP_B7/SRCCLKREQ2*	
TP_PCIE_CLK100M_TBT_BN	J38	CLKOUT_PCIE_N3	
TP_PCIE_CLK100M_TBT_BP	G38	CLKOUT_PCIE_P3	
AP_CLKREQ_L	AV5	GPP_B8/SRCCLKREQ3*	
PCIE_CLK100M_AP_N	H37	CLKOUT_PCIE_N4	
PCIE_CLK100M_AP_P	F37	CLKOUT_PCIE_P4	
CAMERA_CLKREQ_L	AV7	GPP_B9/SRCCLKREQ4*	
PCIE_CLK100M_CAMERA_N	H39	CLKOUT_PCIE_N5	
PCIE_CLK100M_CAMERA_P	F39	CLKOUT_PCIE_P5	
TP_PCH_CLKREQ5_L	BC5	GPP_B10/SRCCLKREQ5*	
SSD_CLKREQ_L	BB10	GPP_B5/SRCCLKREQ0*	

CLKOUT_ITPXDP_N	J34	TP_ITPXDP_CLK100MN	
CLKOUT_ITPXDP_P	G34	TP_ITPXDP_CLK100MP	
GPD8/SUSCLK	BA15	PM_CLK32K_SUSCLK_R	
XTAL24_IN	M1	SYSCLK_CLK24M_PCH	
XTAL24_OUT	L2	NC_PCH_CLK24M_XTALOUT	
XCLK_BIASREF	P1	PCH_DIFFCLK_BIASREF	
RTCX1	BN19	SYSCLK_CLK32K_PCH	
RTCX2	BP18	NC	
SRTCRST*	BH18	PCH_SRTCRST_L	
RTCRST*	BN12	PCH_RTCRST_L	

PP1V_SUS
PLACE_NEAR=U0500.P1:2.54mm
R1662 2.7K 1% 1/20W MF 201

PPVRTC_G3H
R1670 20K 1% 1/20W MF 201
R1671 20K 1% 1/20W MF 201

C1670 1.0UF 20% 6.3V X5R 0201-1
C1671 1.0UF 20% 6.3V X5R 0201-1

PP3V3_SUS
PP3V3_SUS
PP3V3_S0

R1611	100K	5% 1/32W MF 01005	SMC_RUNTIME_SCI_L
R1630	100K	5% 1/32W MF 01005	XDP_USB_EXTA_OC_L
R1631	100K	5% 1/32W MF 01005	USB_EXTB_OC_L
R1632	100K	5% 1/32W MF 01005	XDP_USB_EXTC_OC_L
R1633	100K	5% 1/32W MF 01005	XDP_USB_EXTD_OC_L
R1640	100K	5% 1/32W MF 01005	XDP_JTAG_ISP_TCK
R1641	100K	5% 1/32W MF 01005	XDP_JTAG_ISP_TDI
R1650	47.0K	5% 1/32W MF 01005	TBT_X_CLKREQ_L
R1651	47.0K	5% 1/32W MF 01005	TEST_CLKREQ_L
R1652	47.0K	5% 1/32W MF 01005	AP_CLKREQ_L
R1653	47.0K	5% 1/32W MF 01005	CAMERA_CLKREQ_L
R1655	47.0K	5% 1/32W MF 01005	SSD_CLKREQ_L

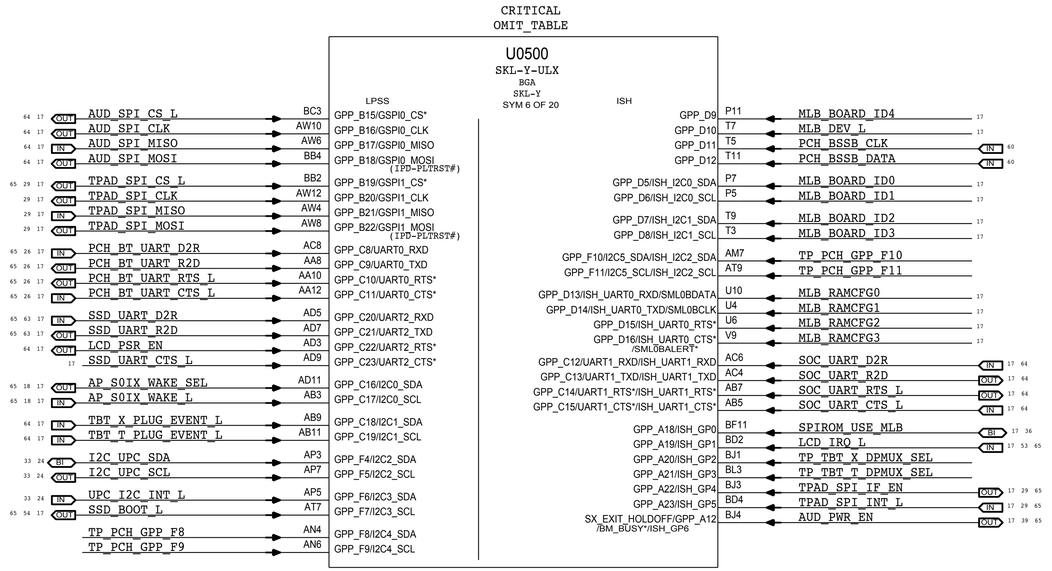
BOM_COST_GROUP=CPU & CHIPSET

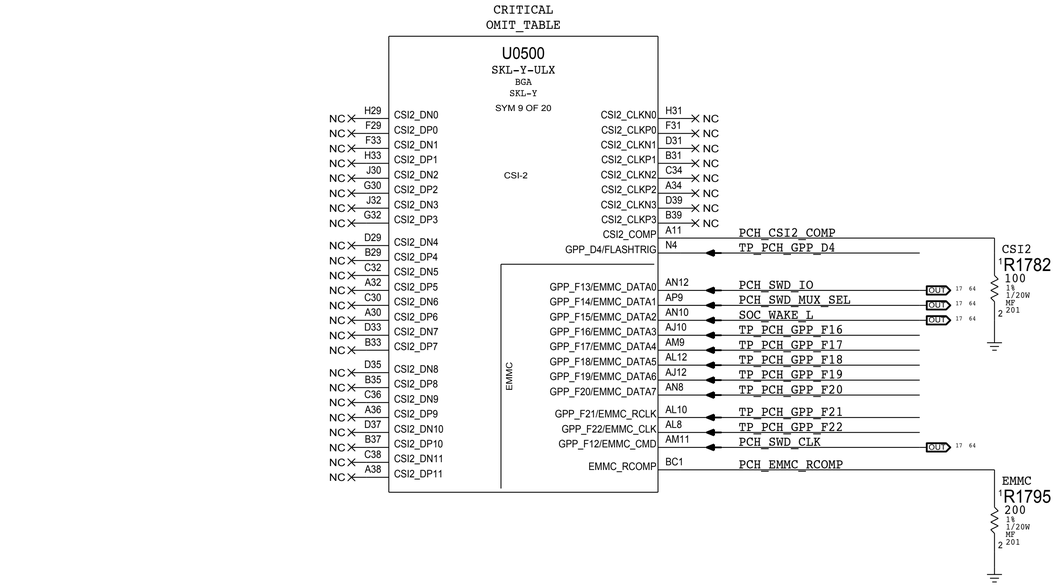
SYNC_MASTER=DEVMLB SYNC_DATE=05/11/2015

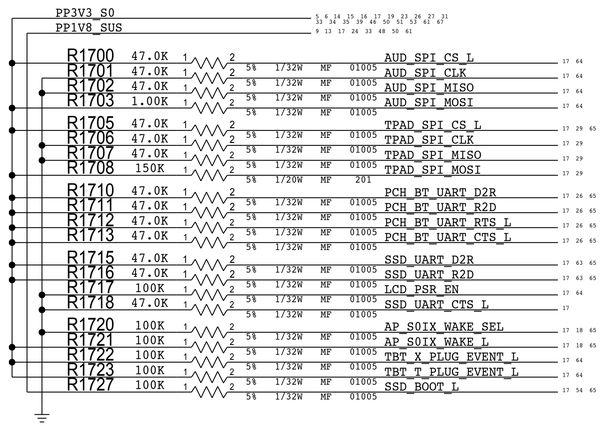
PAGE TITLE
PCH PCIe/USB/CLK

Apple Inc.

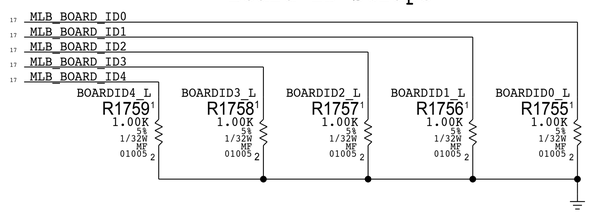
DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 16 OF 130
SHEET 16 OF 67



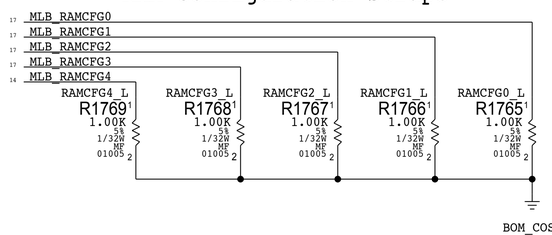


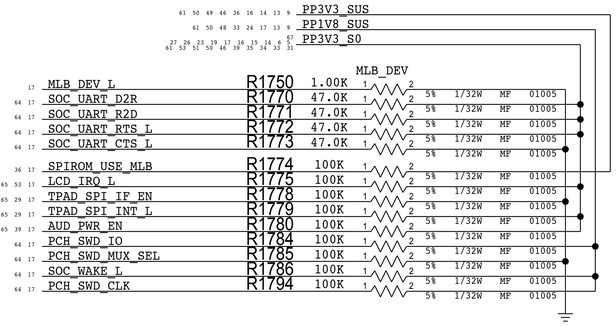


Board ID Straps



RAM Configuration Straps





BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=DEVMLB SYNC_DATE=05/11/2015

PAGE TITLE

PCH GPIO/LPSS

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

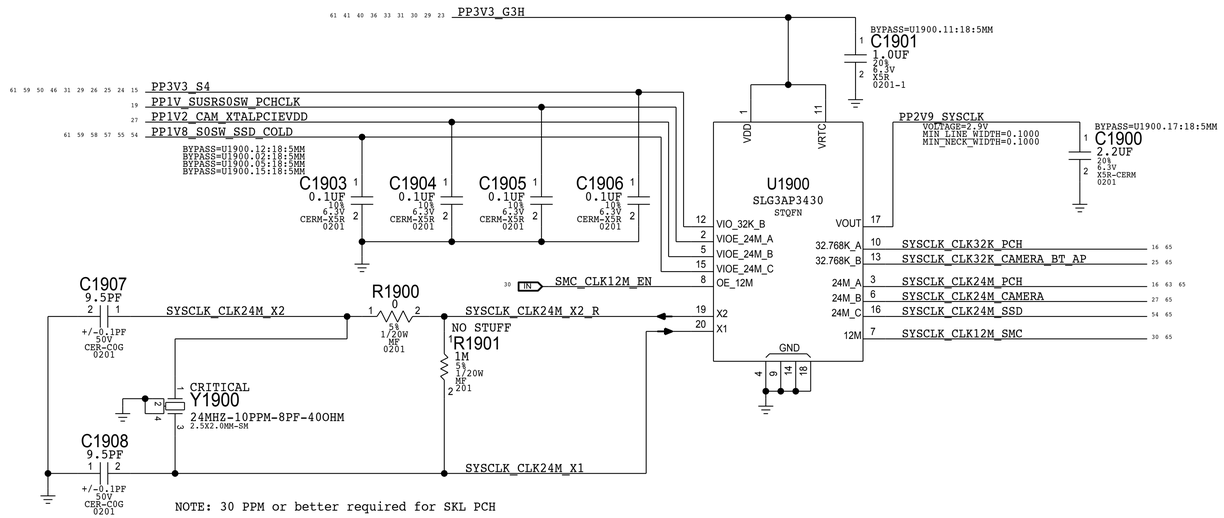
REVISION <E4LABEL>

BRANCH <BRANCH>

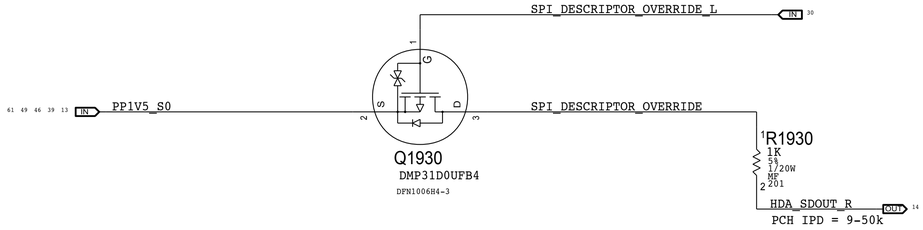
PAGE 17 OF 130

SHEET 17 OF 67

System 32kHz / 12MHz / 24MHz Clock Generator

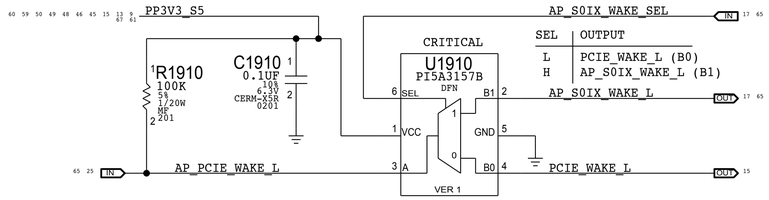


PCH ME Disable Strap



PCH uses HDA_SDO as a power-up strap. If low, ME functions normally.
If high, ME is disabled. This allows for full re-flashing of SPI ROM.
SMC controls strap enable to allow in-field control of strap setting.
***** Circuit does not support HDA voltage >3.3V.

PCIe Wake Muxing

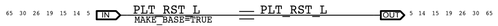


BOM_COST_GROUP=CPU & CHIPSET

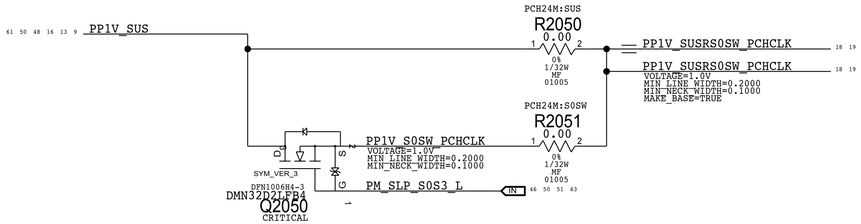
PAGE TITLE	Chipset Support 1
	Apple Inc.
DRAWING NUMBER	<SCH_NUM>
SIZE	D
REVISION	<E4LABEL>
BRANCH	<BRANCH>
PAGE	19 OF 130
SHEET	18 OF 67

Platform Reset Connections

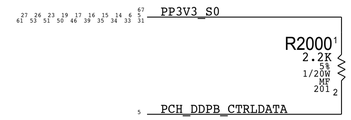
Unbuffered



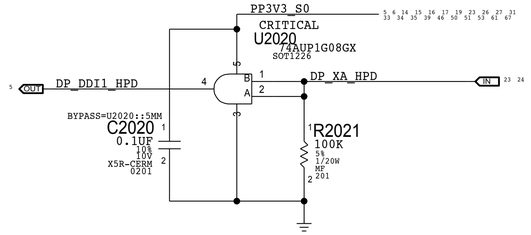
PCH 24MHz VIOE Options



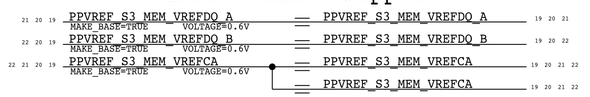
DP DDP Straps



HPD S0 Isolation



LPDDR3 Alias Support



SYNC_MASTER=X260_ERIC SYNC_DATE=06/09/2015

PAGE TITLE

Project Chipset Support

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

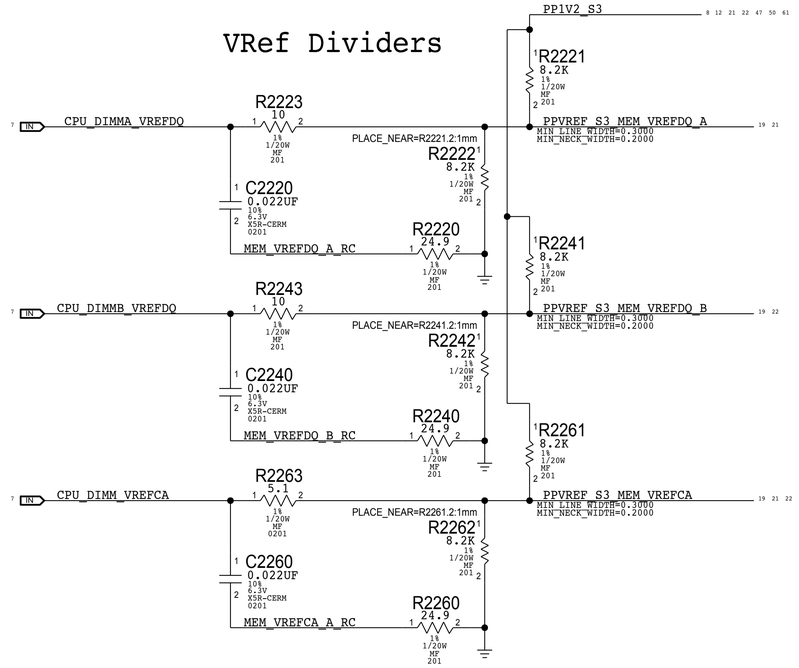
REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 20 OF 130

SHEET 19 OF 67

CPU-Based Margining



SYNC_MASTER=DEVMLB SYNC_DATE=04/14/2015

PAGE TITLE

LPDDR3 VREF MARGINING

Apple Inc.

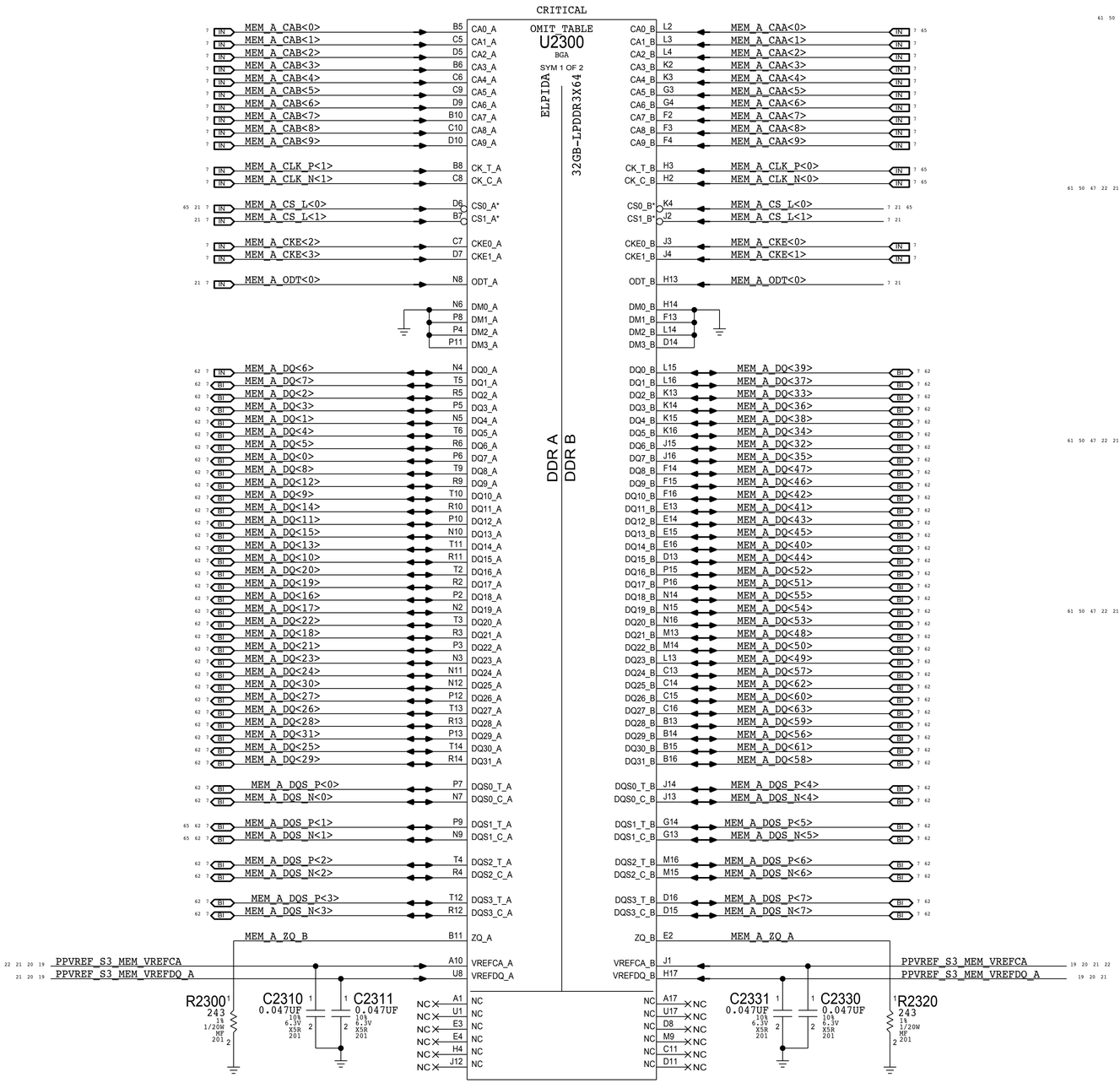
DRAWING NUMBER <SCH_NUM> SIZE D

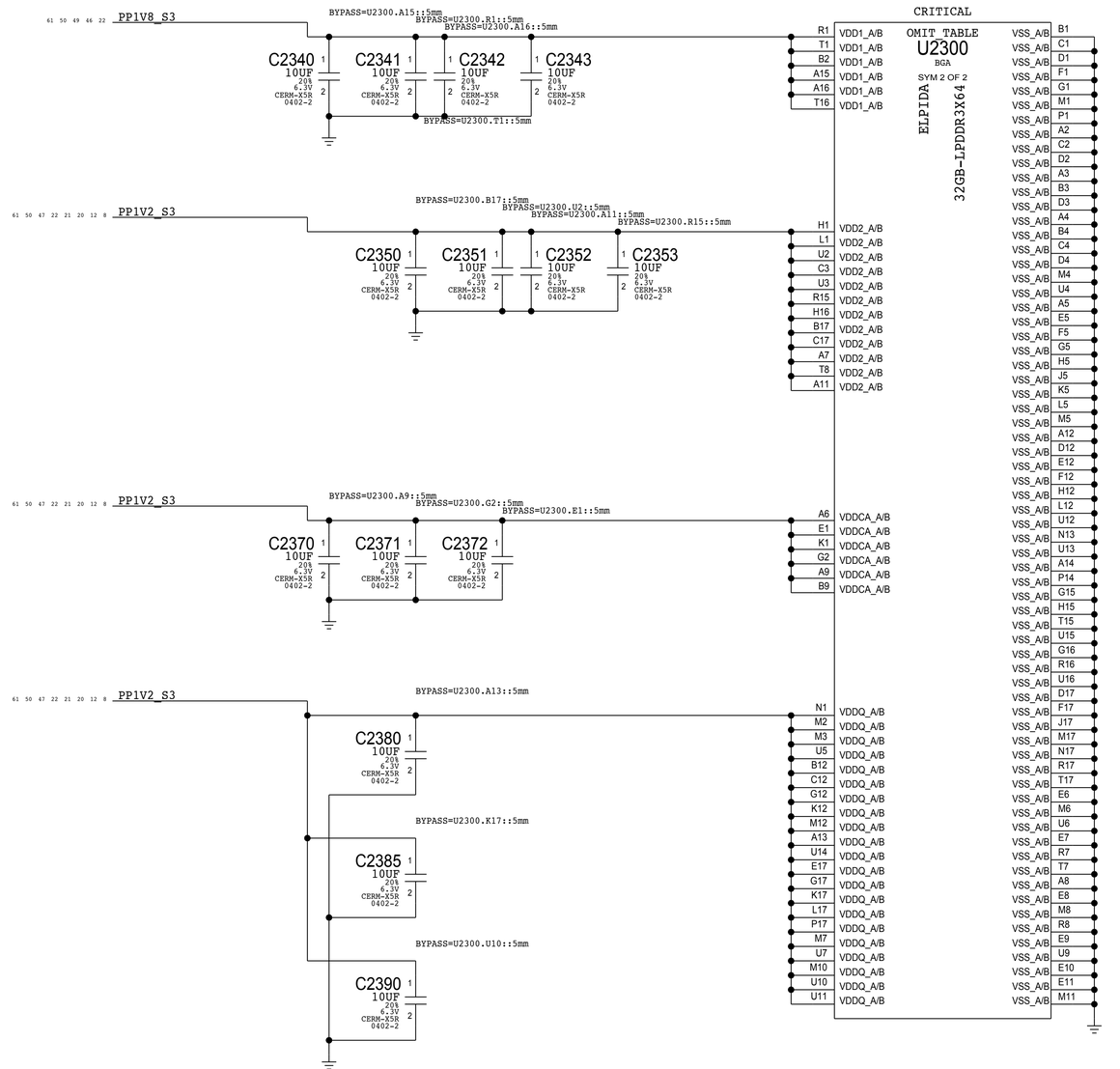
REVISION <E4LABEL>

BRANCH <BRANCH>

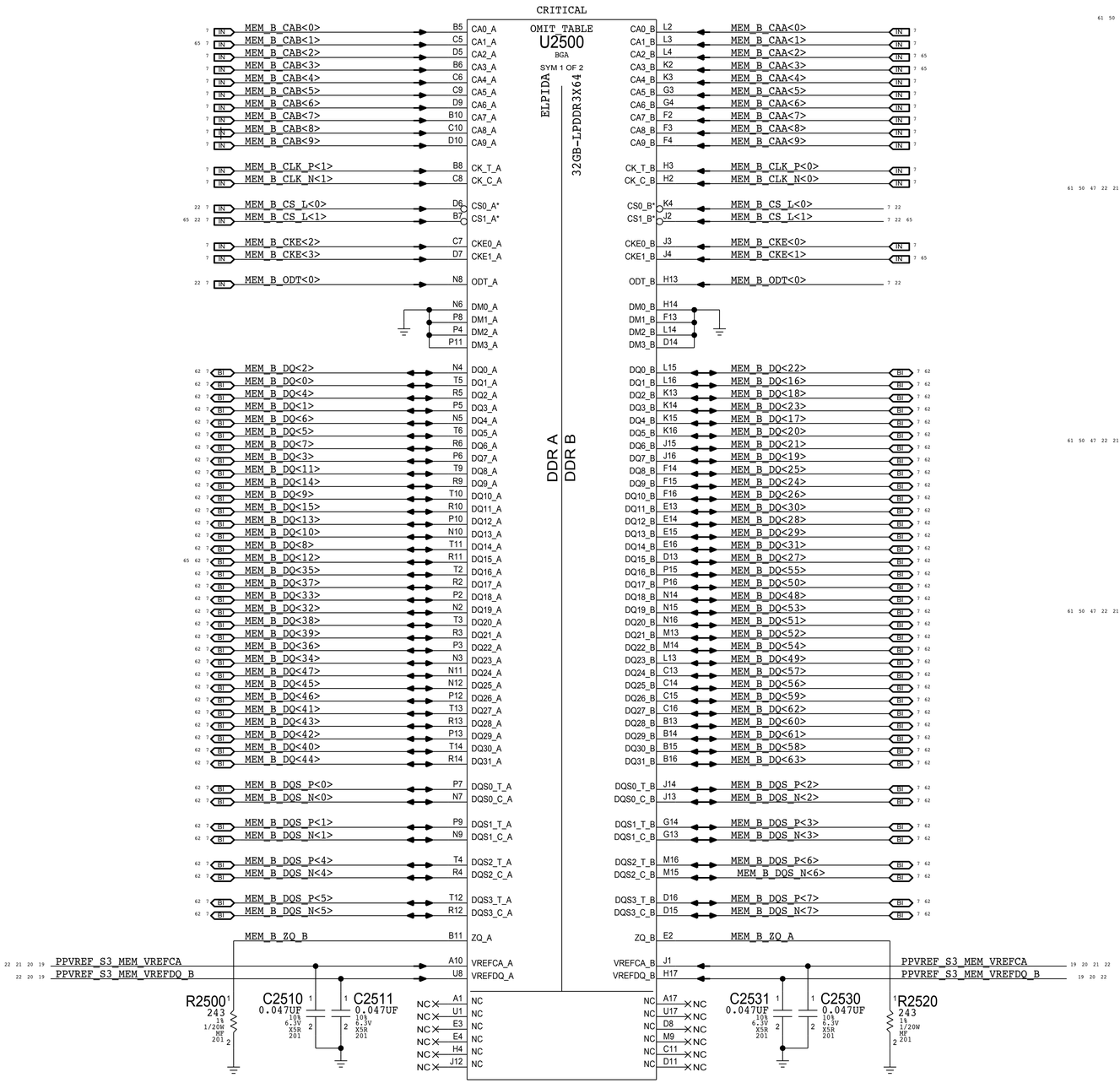
PAGE 22 OF 130

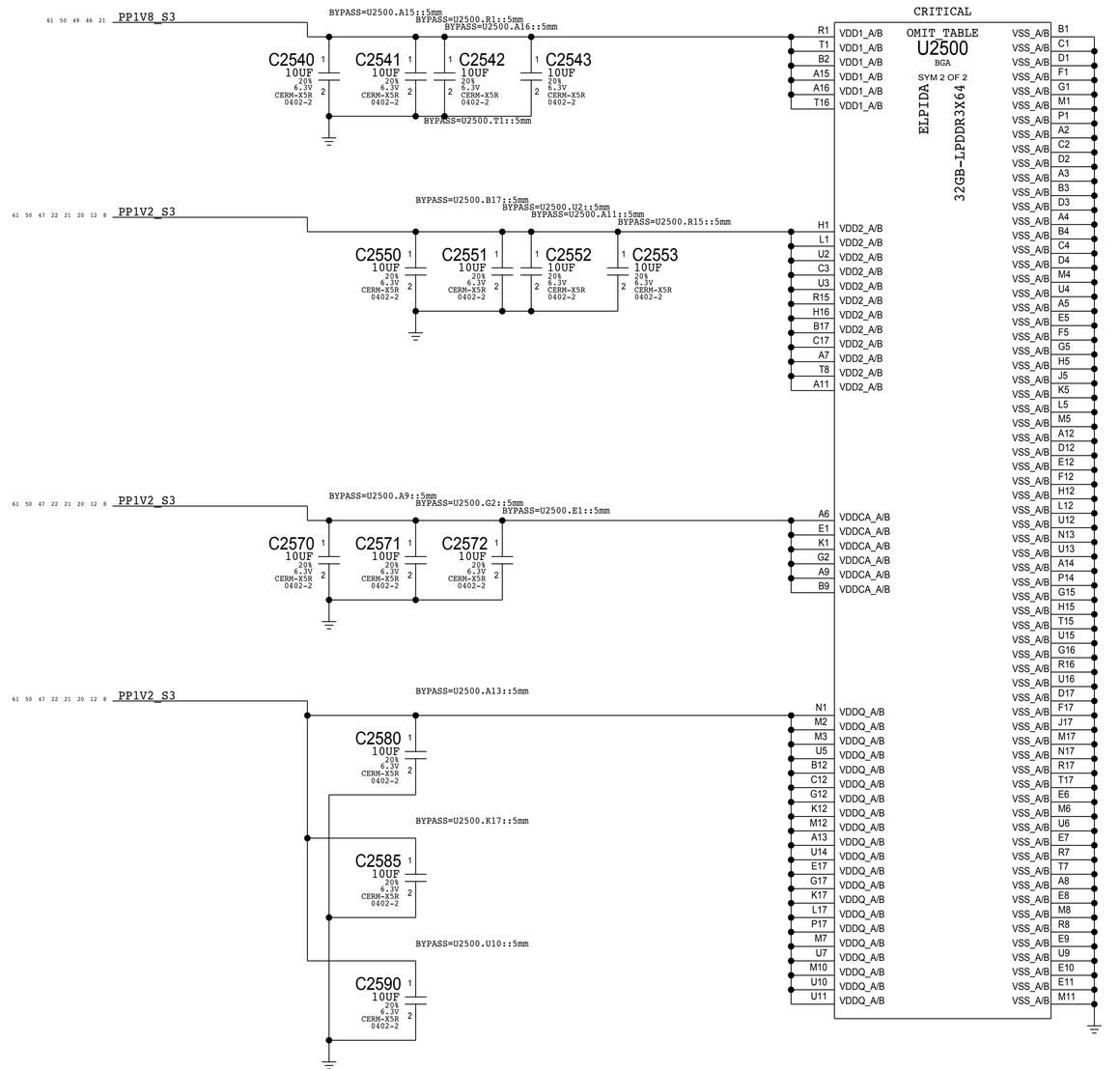
SHEET 20 OF 67





SYNC_MASTER=DEVMLB	SYNC_DATE=04/14/2015
PAGE TITLE	LPDDR3 DRAM Channel A (0-63)
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
	PAGE 23 OF 130
	SHEET 21 OF 67





SYNC_MASTER=DEVMLB SYNC_DATE=04/14/2015

PAGE TITLE

LPDDR3 DRAM Channel B (0-63)

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

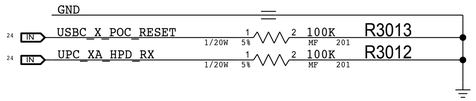
REVISION <E4LABEL>

BRANCH <BRANCH>

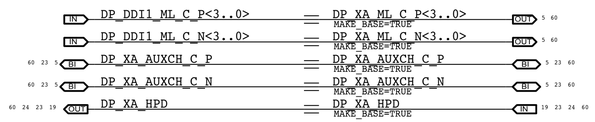
PAGE 25 OF 130

SHEET 22 OF 67

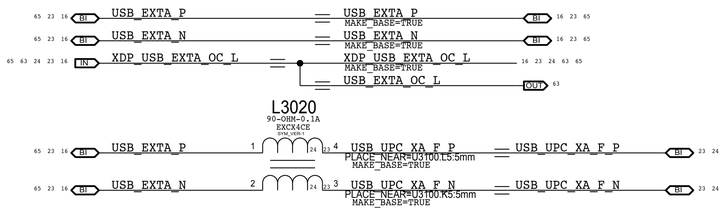
'Ridge-less Support



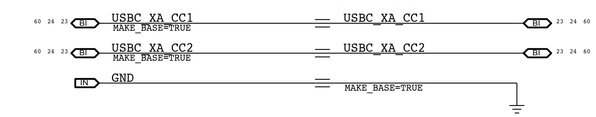
DP Support



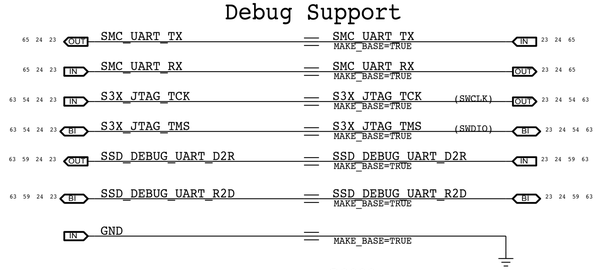
USB Support

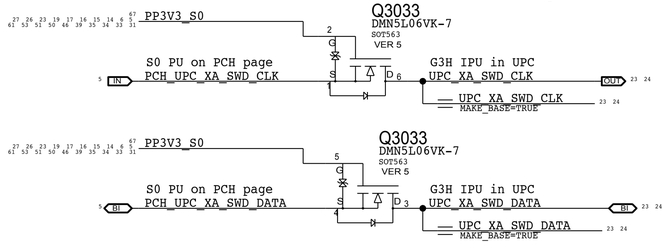


Dead Battery Support

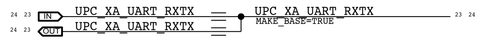


Debug Support

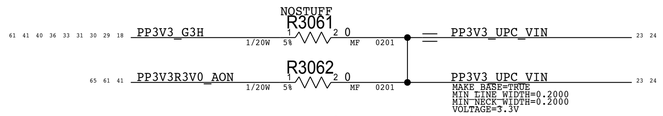




Single Port Support

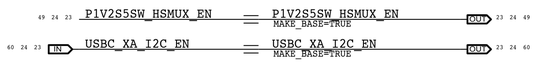


Bring Up Support

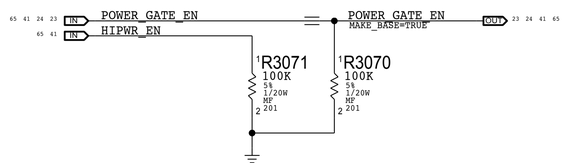


VIN_3V3 power currently required to drive POWER_GATE_EN high. Future OTP update may enable usage of 3V3_G3H instead.

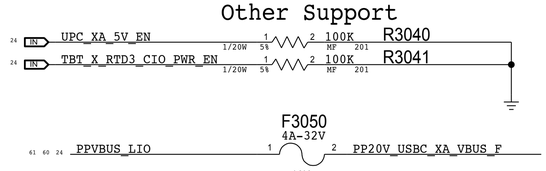
High Speed Mux Support



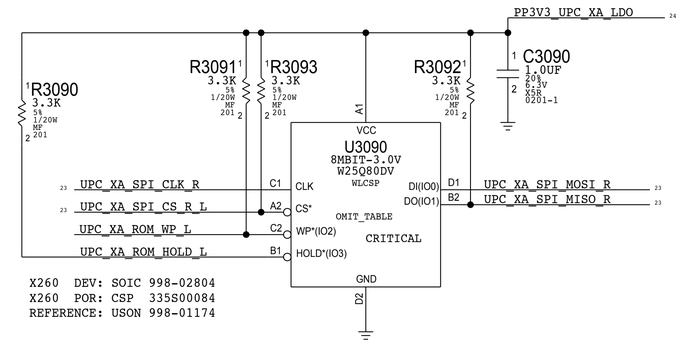
Bansuri Support



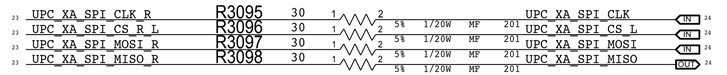
Other Support



Port Controller ROM



X260 DEV: SOIC 998-02804
X260 POR: CSP 335S00084
REFERENCE: USON 998-01174



Place series R at T with dev debug header
Characterize series R on P0 Dev, hopefully remove for P0 POR

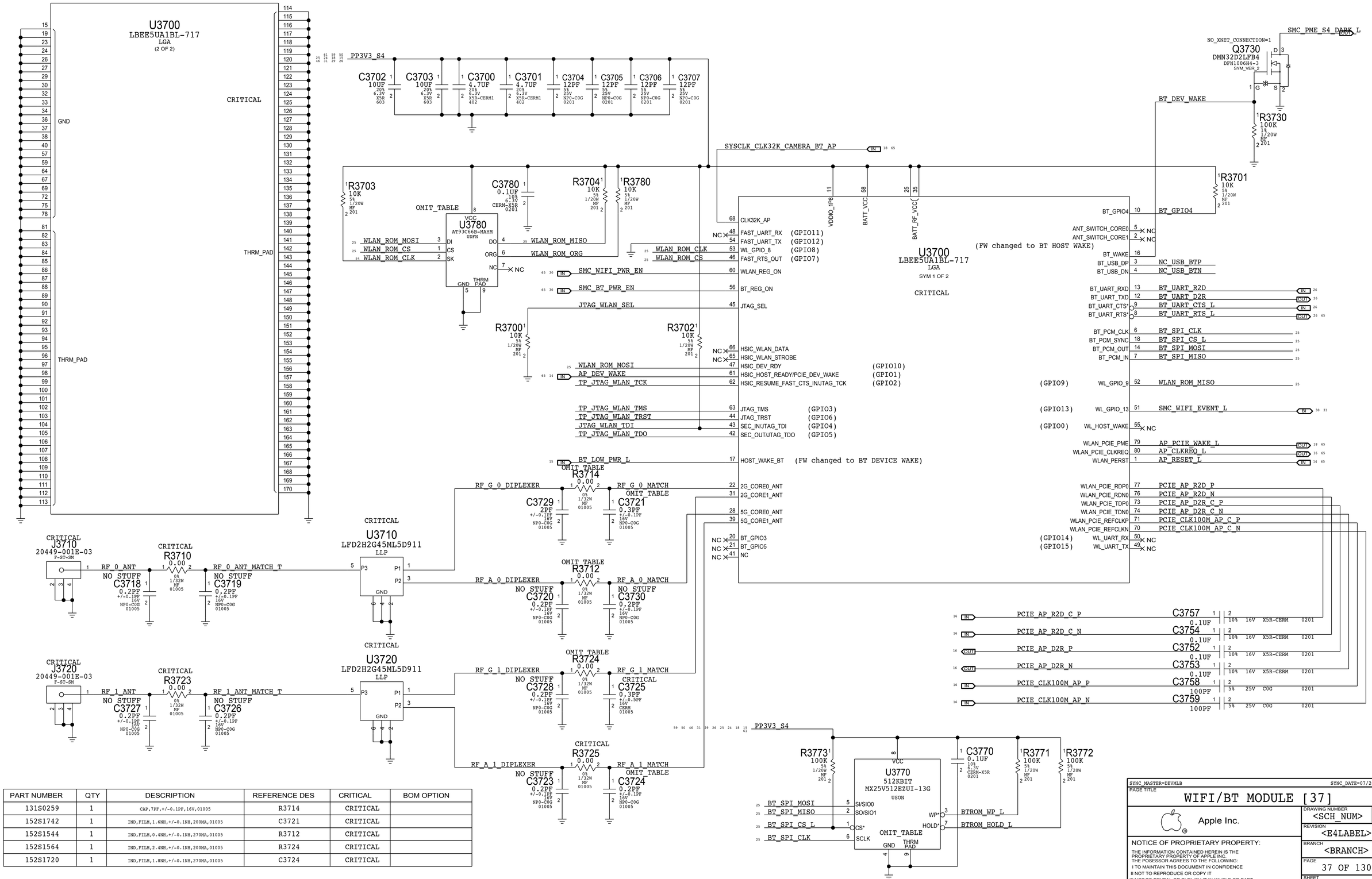
SYNC_MASTER=X260_ERIC	SYNC_DATE=06/04/2015
PAGE TITLE	USB-C Port Controller Support
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
	PAGE 30 OF 130
	SHEET 23 OF 67

PRIMARY ACE USB-C PORT CONTROLLER (UPC)

BOM_COST_GROUP=USB-C

PAGE TITLE	USB-C PORT CONTROLLER A
DRAWING NUMBER	<SCH_NUM>
SIZE	D
REVISION	<E4LABEL>
BRANCH	<BRANCH>
PAGE	31 OF 130
SHEET	24 OF 67

Apple Inc.



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
131S0259	1	CAP,7PF,+/-0.1PF,16V,01005	R3714	CRITICAL	
152S1742	1	IND,FILM,1.6NH,+/-0.1NH,200MA,01005	C3721	CRITICAL	
152S1544	1	IND,FILM,0.4NH,+/-0.1NH,270MA,01005	R3712	CRITICAL	
152S1564	1	IND,FILM,2.4NH,+/-0.1NH,200MA,01005	R3724	CRITICAL	
152S1720	1	IND,FILM,1.8NH,+/-0.1NH,270MA,01005	C3724	CRITICAL	

SYNC_MASTER=DEVMLB SYNC_DATE=07/20/2015

PAGE TITLE

WIFI/BT MODULE [37]

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

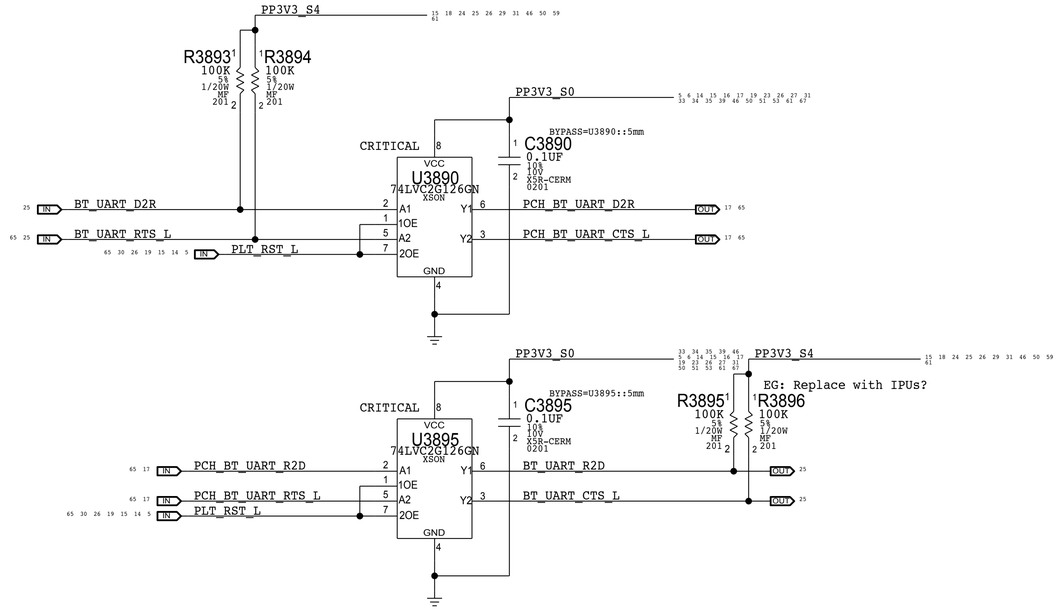
REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 37 OF 130

SHEET 25 OF 67

BT UART Isolation



SYNC_MASTER=J92_DEVMLB SYNC_DATE=05/13/2015

PAGE TITLE

WIFI/BT Support

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 38 OF 130

SHEET 26 OF 67

U3900
BCM15700A2KFEB4G
FBGA
SYM 3 OF 3
CRITICAL

L3902
1.0UH-1.6A-55MOHM
PLACE_NEAR=U3900.K13:4MM
BYPASS=U3900.K13::2.54MM

L3901
1.0UH-1.6A-55MOHM
PLACE_NEAR=U3900.M13:4MM
PLACE_NEAR=U3900.M13:2.54MM

L3903
220-OHM-1.4A

L3904
220-OHM-1.4A

L3906
22NH

PP1V35_CAM
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2000
VOLTAGE=1.35V

PP1V35_DDR_CLK
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2000
VOLTAGE=1.35V

PP0V675_CAM_VREF
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2000
VOLTAGE=0.675V

PP1V2_CAM_PCIE_VDD_FLT
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2000
VOLTAGE=1.2V

PP1V2_CAM_PCIE_PVDD_FLT
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2000
VOLTAGE=1.2V

(=PP3V3_S0_CAMERA)

GND_CAM_PVSSC
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2000
VOLTAGE=0V

P1V2_CAM_SRVLXC_PHASE
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2000
DIDT=TRUE

P1V35_CAM_SRVLXD_PHASE
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2000
DIDT=TRUE

PP1V35_CAM

PP1V8_CAM
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2000
VOLTAGE=1.8V

PP1V2_CAM
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2000
VOLTAGE=1.2V

PP1V2_CAM_XTALPCIEVDD
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2000
VOLTAGE=1.2V
MAKE_BASE=TRUE

PP3V3_S0

GND_CAM_PVSSD

GND_CAM_PVSSC

XW3900
XW3901

L3901:1 VSENSE_C
L3902:1 VSENSE_D

MIPI_AGND
PCIE_GND
PMU_AVSS
SR_PVSSC
SR_PVSSD
VSSC
XTAL_AVSS

DDR_VDDIO
DDR_VDDIO_CK
DDR_VREF
PCIE_VDD1P2
PCIE_PVDD1P2
DDR_AVDD1P8
MIPI_AVDD1P8
PLL_VDD1P8
OTP_VDD3P3
SR_VDD_3P3C
SR_VDD_3P3D
SR_VLXC_O
SR_VLXD_O
VDD_1P35A
VDD_3P3A
VDD1P2_O
VDD1P8_O
VDDC
VDDO18
XTAL_AVDD1P2

U3900
BCM15700A2KFEB4G
FBGA
SYM 2 OF 3
CRITICAL

DDR_AD00 … DDR_AD14
DDR_BA0 … DDR_BA2
DDR_CK_P0 DDR_CK_N0
DDR_DM0 DDR_DM1
DDR_ZQ DDR_CKE DDR_CS*
DDR_DQ00 … DDR_DQ15
DDR_DQS_P0 DDR_DQS_N0
DDR_DQS_P1 DDR_DQS_N1
DDR_RAS* DDR_WE* DDR_CAS* DDR_RESET*

U3900
BCM15700A2KFEB4G
FBGA
SYM 1 OF 3
CRITICAL

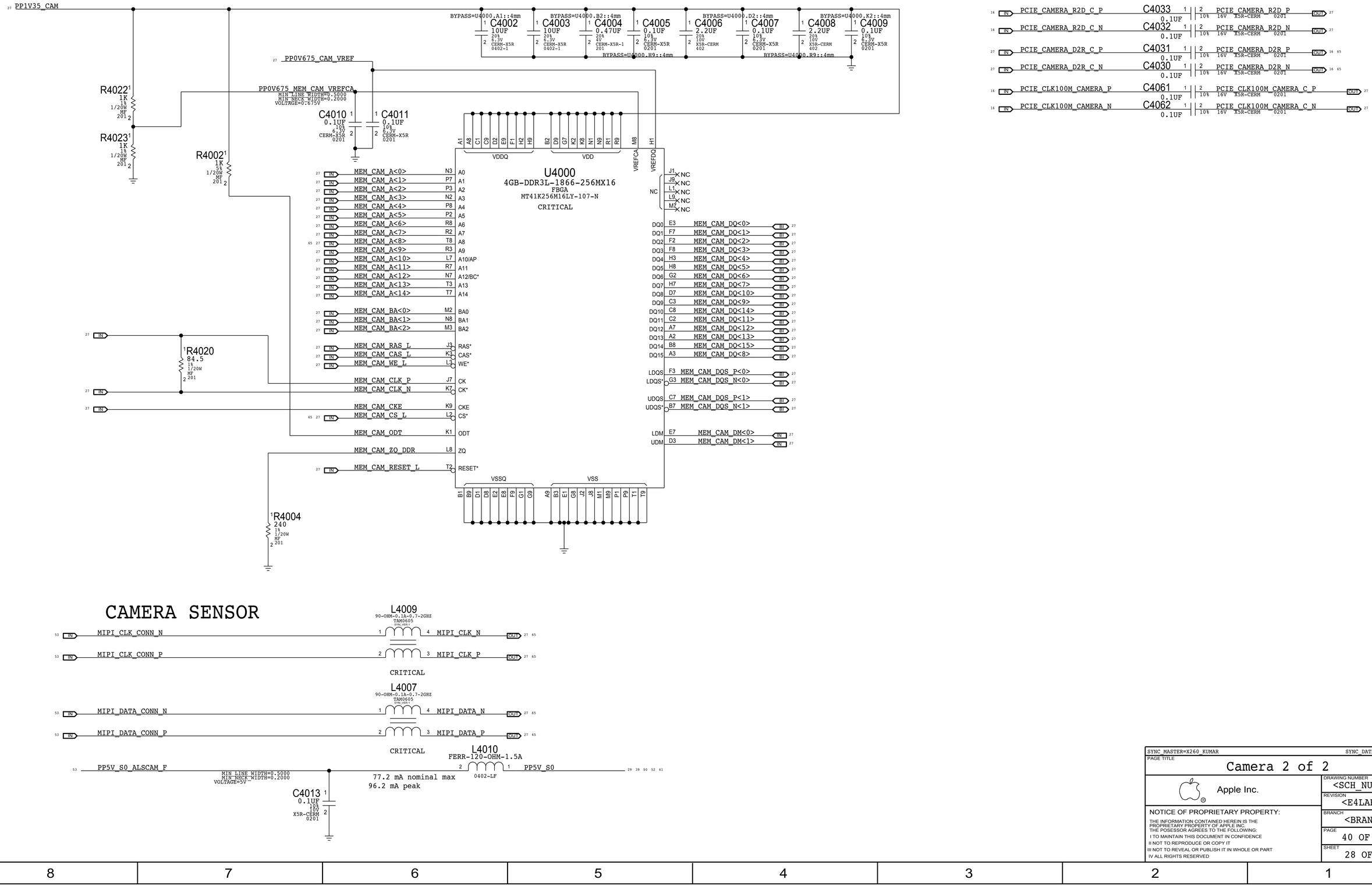
MIPI_CLK_P MIPI_CLK_N
MIPI_DATA_P MIPI_DATA_N
MIPI_DP1 MIPI_DM1
PCIE_CAMERA_R2D_P PCIE_CAMERA_R2D_N
PCIE_CLK100M_CAMERA_C_P PCIE_CLK100M_CAMERA_C_N
PCIE_CAMERA_D2R_C_P PCIE_CAMERA_D2R_C_N
PCIE_TESTP PCIE_TESTN
SYSCLK_CLK24M_CAMERA CLK25M_CAM_CLKN
I2C_CAM_SMBDBG_CLK I2C_CAM_SCK
I2C_CAM_SMBDBG_DAT I2C_CAM_SDA
TP_CAM_JTAG_TCK TP_CAM_JTAG_TDI TP_CAM_JTAG_TDO TP_CAM_JTAG_TMS TP_CAM_JTAG_TRST_L TP_CAM_JTAG_SRST_L
CAMERA_CLKREQ_L CAMERA_RESET_L TP_CAM_PCIE_WAKE_L
CAM_PWR_SEL CAM_DEBUG_RESET_L
CAM_SENSOR_WAKE_L CAMERA_PWR_EN
PU on PCH page

DEBUG_00 … DEBUG_16
GPIO_00 … GPIO_07
UARTCTS UARTRTS UARTRXD UARTTXD
TEST_OUT TEST_MODE
STRAP_XTAL_FREQ STRAP_XTAL_SEL

CAM_FREQ:25M
PU = 25MHz
CAM_FREQ:24M
PD = 24MHz
CAM_XTAL:YES
CAM_XTAL:NO
CAM_XTAL_FREQ
CAM_XTAL_SEL

CAM_UARTCTS
CAM_UARTRXD
CAM_TEST_MODE
CAM_TEST_OUT
NO STUFF

SYNC_MASTER=X260_ERIC
SYNC_DATE=06/04/2015
PAGE TITLE
Camera 1 of 2
Apple Inc.
DRAWING NUMBER <SCH_NUM>
SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 39 OF 130
SHEET 27 OF 67



SYNC_MASTER=X260_KUMAR SYNC_DATE=06/16/2015

PAGE TITLE: Camera 2 of 2

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 40 OF 130

SHEET: 28 OF 67

IPD ZIF CONNECTOR

Bottom side contacts used
Pinout reversed from flex

518S0854
CRITICAL
J4801
502250-8041
F-RT-SM

TPAD_SPI_CS_L
TPAD_SPI_IF_EN
SMC_PME_S4_WAKE_L
PP3V3_S4_TPAD_F
TP_USB_TPADN
SMC_ACTUATOR_DISABLE_L
SMBUS_SMC_3_SDA
PP3V3_G3H_KBD_F
PP5V_S0_KBD_F

TPAD_SPI_MISO_R
TPAD_SPI_MOSI_R
TPAD_SPI_CLK_R
TPAD_SPI_INT_L
PP3V3_S4_TPAD_F
TP_USB_TPADP
PP5V_S4_TPAD_F
SMBUS_SMC_3_SCL
SMC_LSOC_RST
SMC_ONOFF_L
PP5V_S0_KBD_F
SMC_LID
TP_USB_VBUS_EN

R4802 15 1/20W MF 201 — TPAD_SPI_MISO
R4801 15 1/20W MF 201 — TPAD_SPI_MOSI
R4803 15 1/20W MF 201 — TPAD_SPI_CLK
R4870 100K 5% 1/20W MF 201

CRITICAL
F4800 3A-6A-9V-0.05OHM 0603
PPBUS_G3H → PPBUS_G3H_TPAD_FUSED
MIN_LINE_WIDTH=0.6000 MIN_NECK_WIDTH=0.1000 VOLTAGE=8.7V

CRITICAL
L4800 30-OHM-5A 0603
PPBUS_G3H_TPAD_FUSED → PPBUS_G3H_TPAD_FLT
MIN_LINE_WIDTH=0.6000 MIN_NECK_WIDTH=0.1000 VOLTAGE=8.7V

C4800 0.1UF 10% 10V X5R-CERM 0201

XW4801 SM — GND_ACTUATOR
MIN_LINE_WIDTH=0.6000 MIN_NECK_WIDTH=0.1000 VOLTAGE=0V

CRITICAL
L4801 FERR-120-OHM-1.5A 0402-LF
PP3V3_G3H_KBD_F → PP3V3_G3H
MIN_LINE_WIDTH=0.5000 MIN_NECK_WIDTH=0.2000 VOLTAGE=3.3V
C4801 0.1UF 10% 10V X5R-CERM 0201

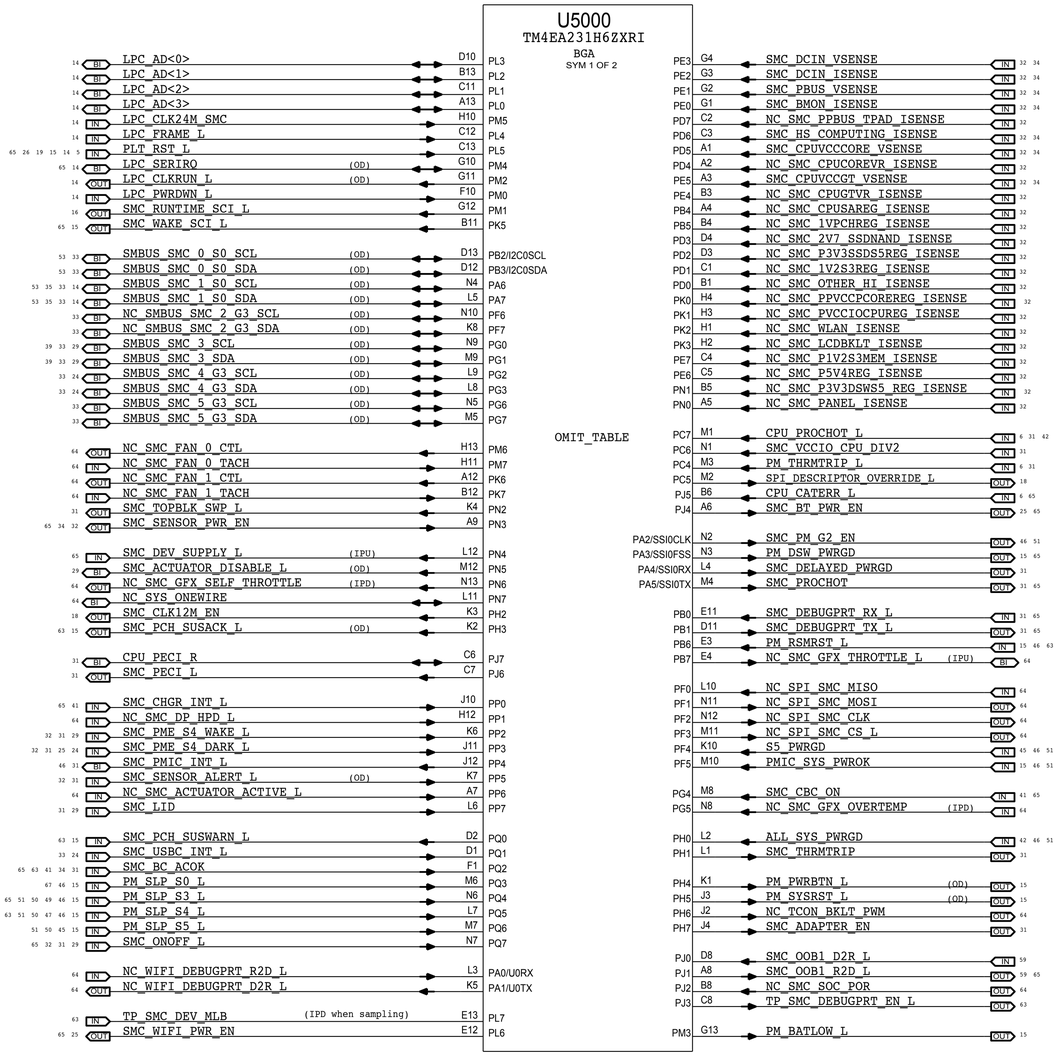
CRITICAL
L4802 FERR-120-OHM-1.5A 0402-LF
PP3V3_S4_TPAD_F → PP3V3_S4
MIN_LINE_WIDTH=0.5000 MIN_NECK_WIDTH=0.2000 VOLTAGE=3.3V
C4802 0.1UF 10% 10V X5R-CERM 0201

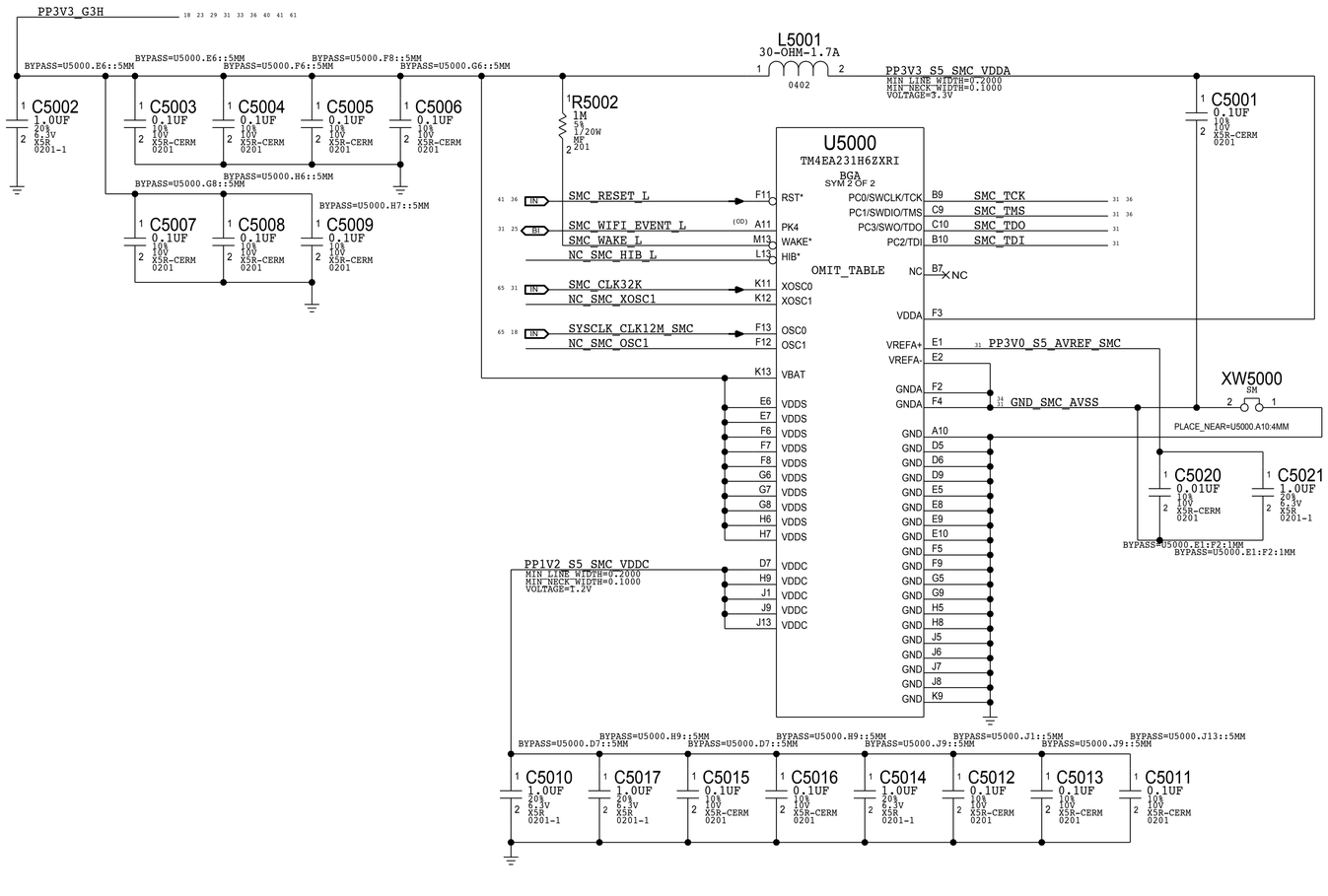
CRITICAL
L4803 FERR-120-OHM-1.5A 0402-LF
PP5V_S4_TPAD_F → PP5V_S4
MIN_LINE_WIDTH=0.5000 MIN_NECK_WIDTH=0.2000 VOLTAGE=5V
C4803 0.1UF 10% 10V X5R-CERM 0201

CRITICAL
L4804 FERR-120-OHM-1.5A 0402-LF
PP5V_S0_KBD_F → PP5V_S0
MIN_LINE_WIDTH=0.5000 MIN_NECK_WIDTH=0.2000 VOLTAGE=5V
C4804 0.1UF 10% 10V X5R-CERM 0201

BYPASS=J4801.20::1.5MM
BYPASS=J4801.22::1.5MM
BYPASS=J4801.26::1.5MM
SMC_LSOC_RST
SMC_ONOFF_L
SMC_LID
C4810 100PF 5% 25V C0G 0201
C4811 100PF 5% 25V C0G 0201
C4812 100PF 5% 25V C0G 0201

SYNC_MASTER=DEVMLB SYNC_DATE=05/11/2015
PAGE TITLE: Keyboard & Trackpad Conn
Apple Inc.
DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 48 OF 130
SHEET: 29 OF 67



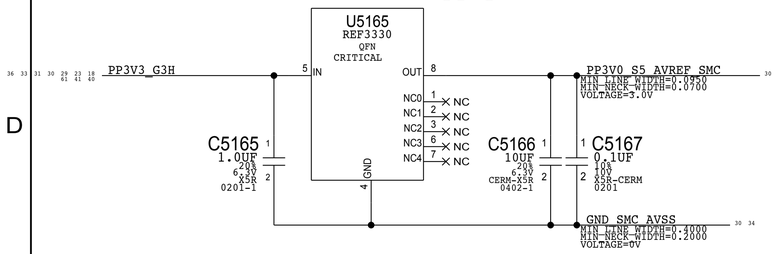


NOTE:
SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

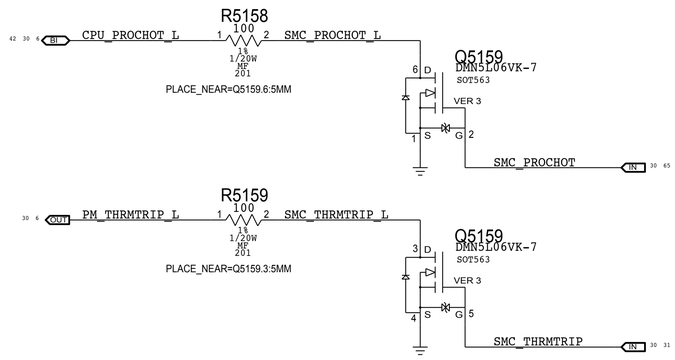
NOTE:
Unused pins have "SMC_Pxx" names. Unused
pins designed as outputs can be left floating,
those designated as inputs require pull-ups.

PAGE TITLE	SMC
	Apple Inc.
DRAWING NUMBER	<SCH_NUM>
SIZE	D
REVISION	<E4LABEL>
BRANCH	<BRANCH>
PAGE	50 OF 130
SHEET	30 OF 67

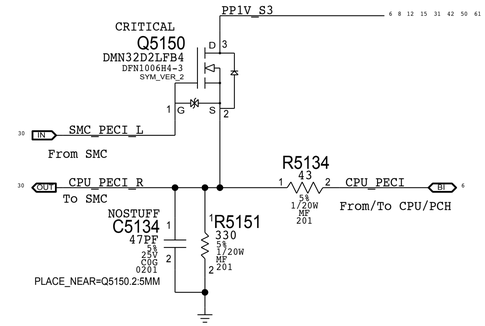
SMC AVREF Supply



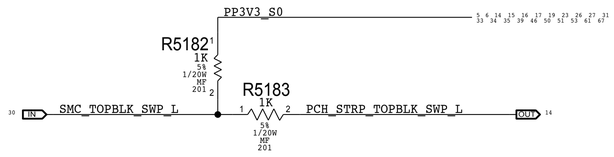
PROCHOT/THRMTRIP Support

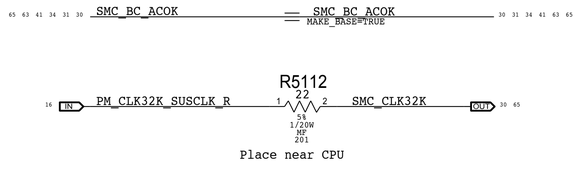


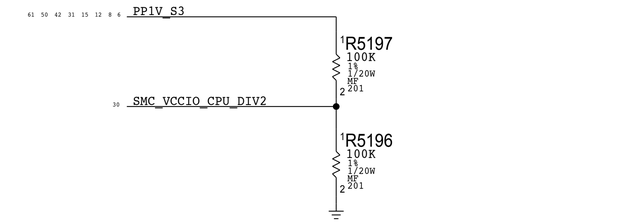
PECI Support

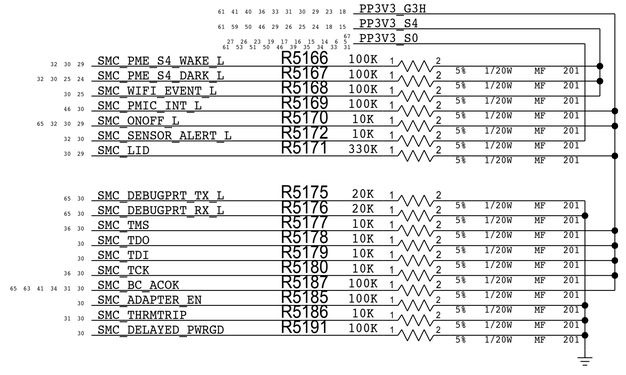


Top-Block Swap









SYNC_MASTER=X260_ERIC SYNC_DATE=06/04/2015

PAGE TITLE

SMC Shared Support

Apple Inc.

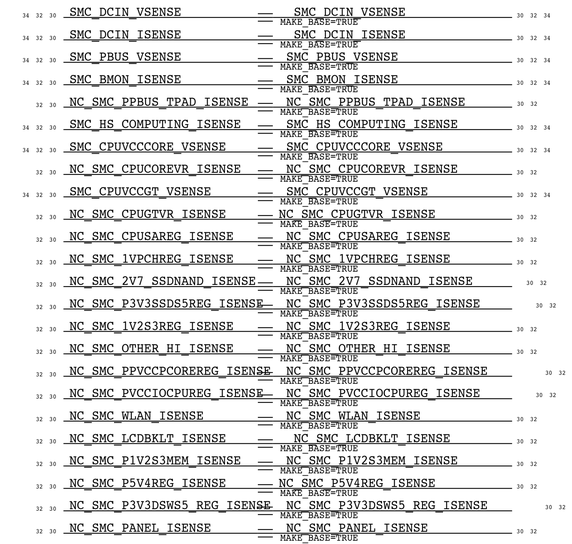
DRAWING NUMBER <SCH_NUM> SIZE D

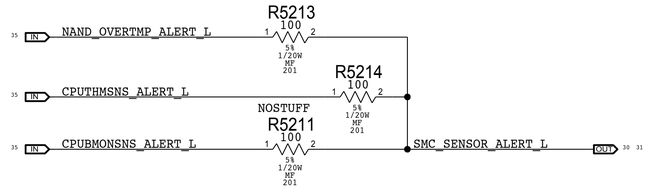
REVISION <E4LABEL>

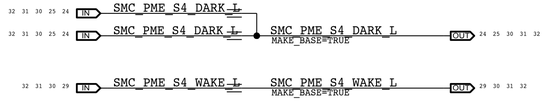
BRANCH <BRANCH>

PAGE 51 OF 130

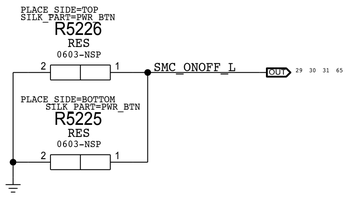
SHEET 31 OF 67







Debug Power "Buttons"



SYNC_MASTER=X26O_ERIC SYNC_DATE=06/04/2015

PAGE TITLE

SMC Project Support

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

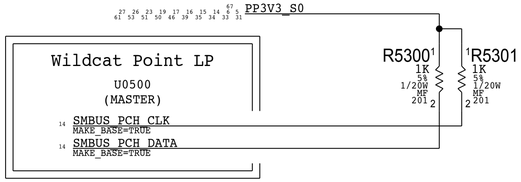
REVISION <E4LABEL>

BRANCH <BRANCH>

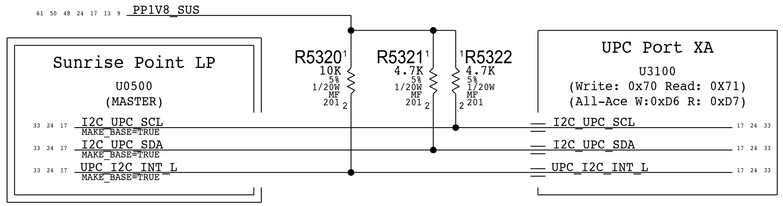
PAGE 52 OF 130

SHEET 32 OF 67

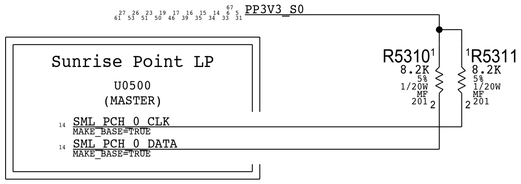
Sunrise Point LP S0 SMBus "0" Connections



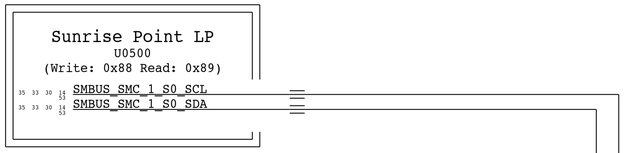
Sunrise Point LP S0 I2C "2" Connections



Sunrise Point LP S0 "SMLink 0" Connections



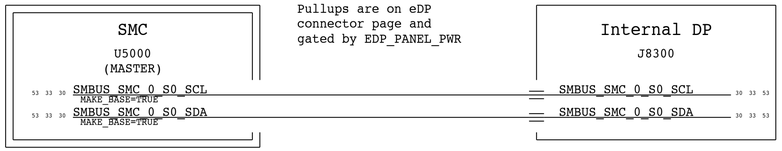
Sunrise Point LP S0 "SMLink 1" Connections



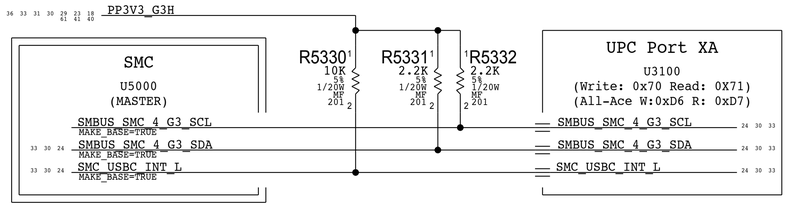
SMLink 1 is slave port to
access PCH

SMC "0" SMBus S0 Connections

Pullups are on eDP
connector page and
gated by EDP_PANEL_PWR

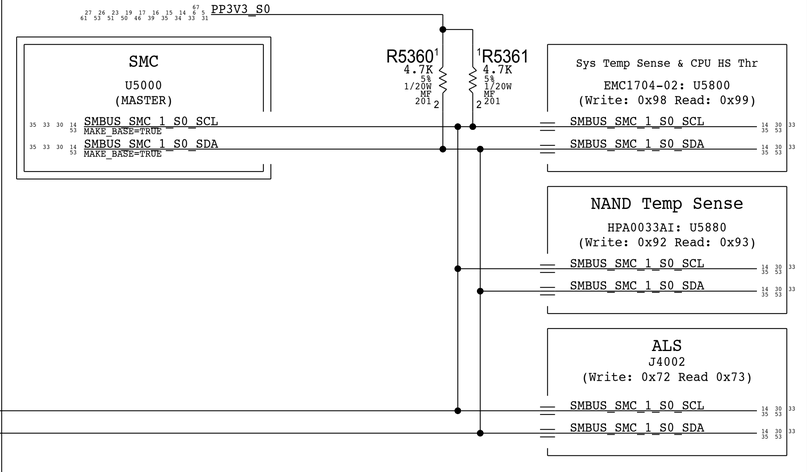


SMC "4" SMBus G3H Connections

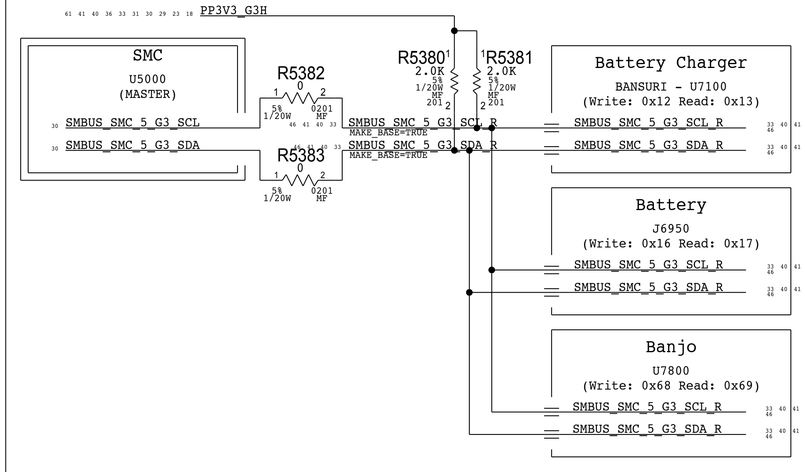


SMC "2" SMBus Connections

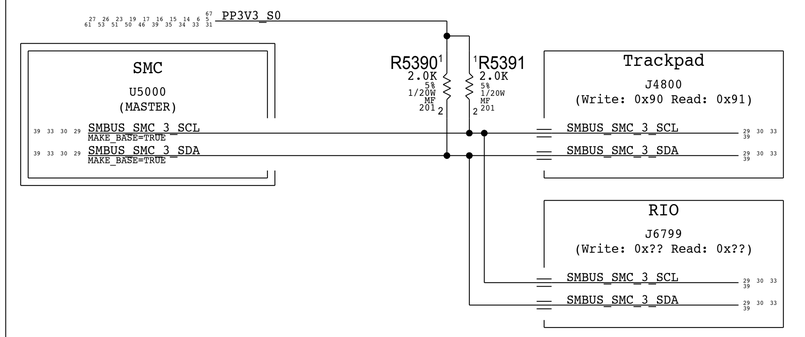
SMC S0 "1" SMBus Connections



SMC "5" SMBus G3H Connections



SMC "3" SMBus S0 Connections



SYNC_MASTER=DEVMLB SYNC_DATE=05/11/2015

PAGE TITLE

SMBus Connections

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

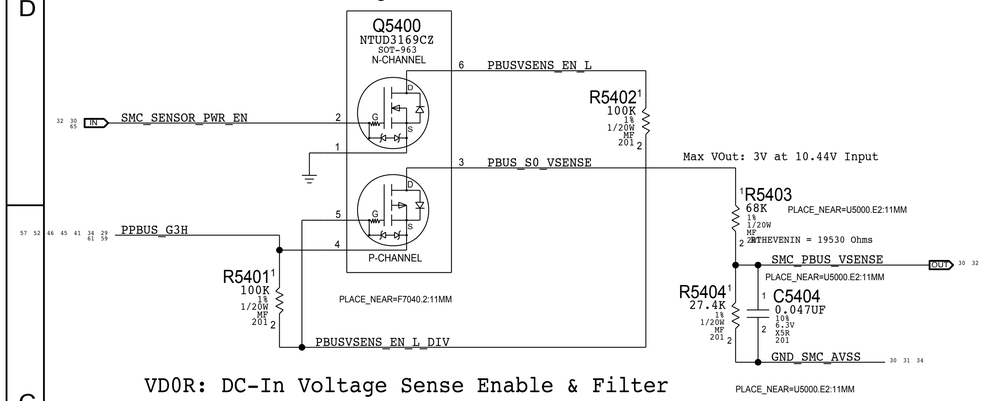
BRANCH <BRANCH>

PAGE 53 OF 130

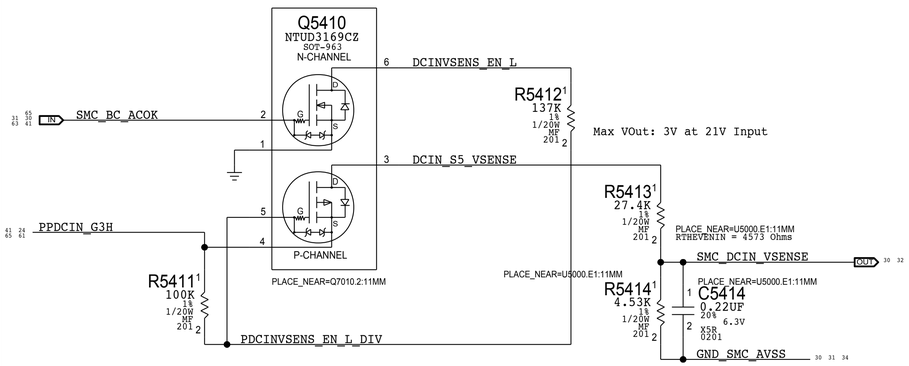
SHEET 33 OF 67

POR VOLTAGE / CURRENT SENSORS : TO BE USED IN PRODUCTION

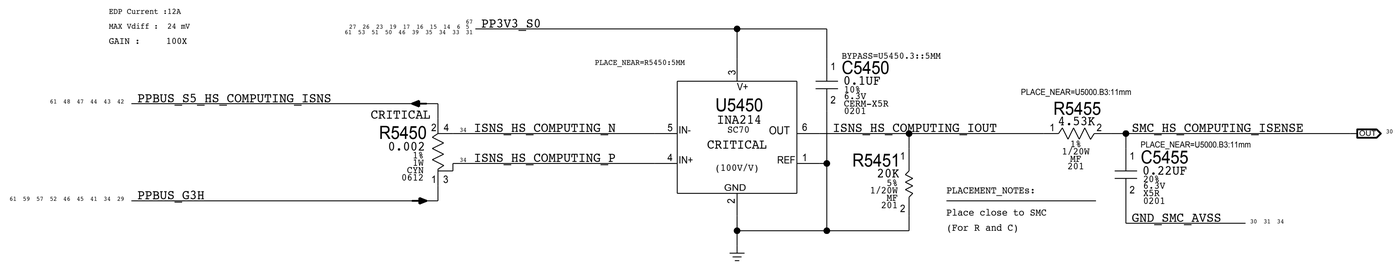
VP0R: PBUS Voltage Sense Enable & Filter



VD0R: DC-In Voltage Sense Enable & Filter

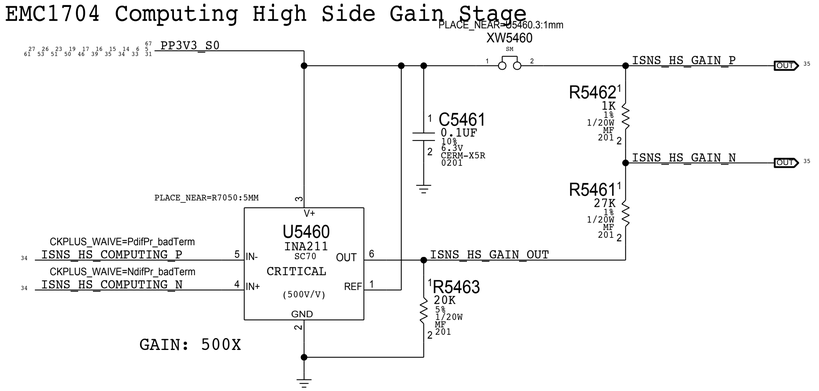


IC0R : COMPUTING High Side Current Sense

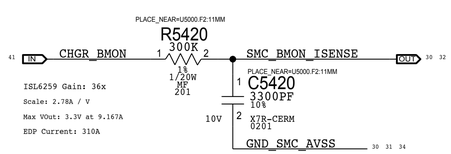


Need to set gains for ULX

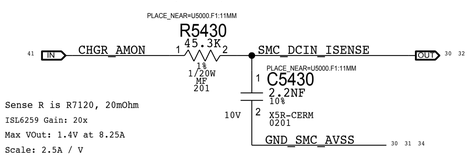
EMC1704 Computing High Side Gain Stage



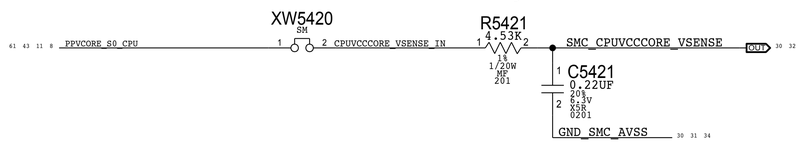
CHARGER BMON High Side Current Sense



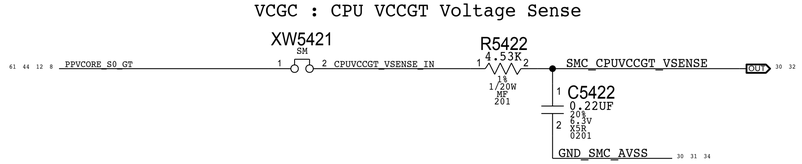
DC-IN (AMON) Current Sense



VC0C : CPU VCC CORE Voltage Sense



VCGC : CPU VCCGT Voltage Sense



SYNC_MASTER=DEVMLB SYNC_DATE=07/06/2015

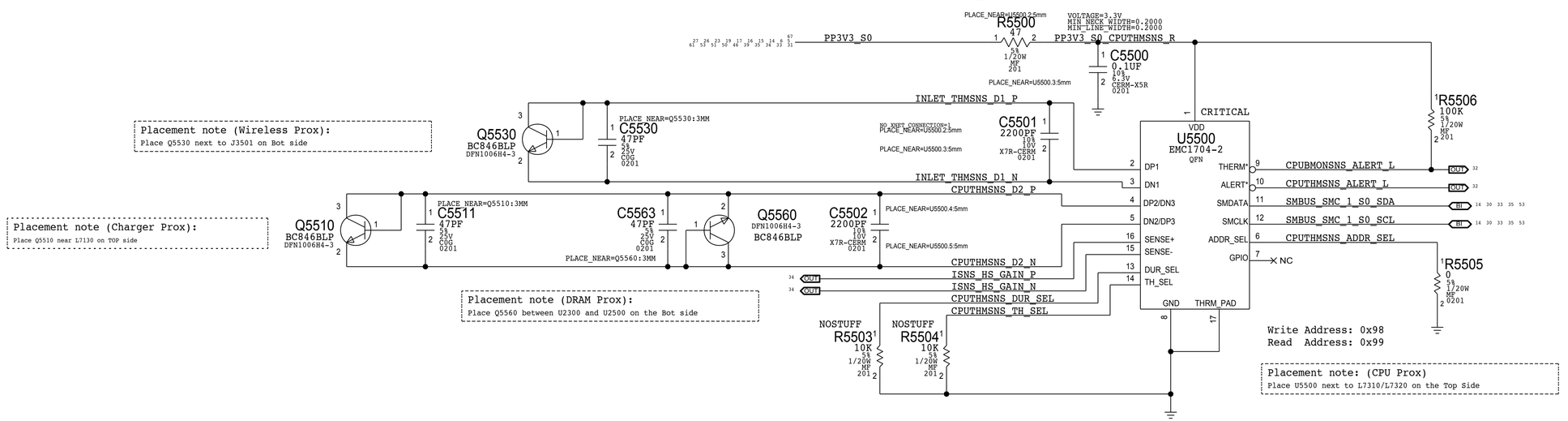
PAGE TITLE: Voltage & Current Sensing

Apple Inc.

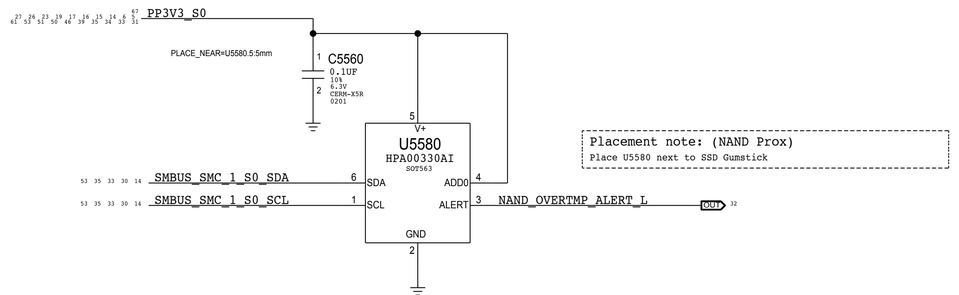
DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 54 OF 130
SHEET: 34 OF 67

POR THERMAL SENSORS : TO BE USED IN PRODUCTION

CPU Proximity, Inlet ,DDR and BMON THR Sensor



NAND Temp Sensor



SENSORS

SYNC_MASTER=X260_KUMAR SYNC_DATE=06/16/2015

PAGE TITLE: Temperature Sensing

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

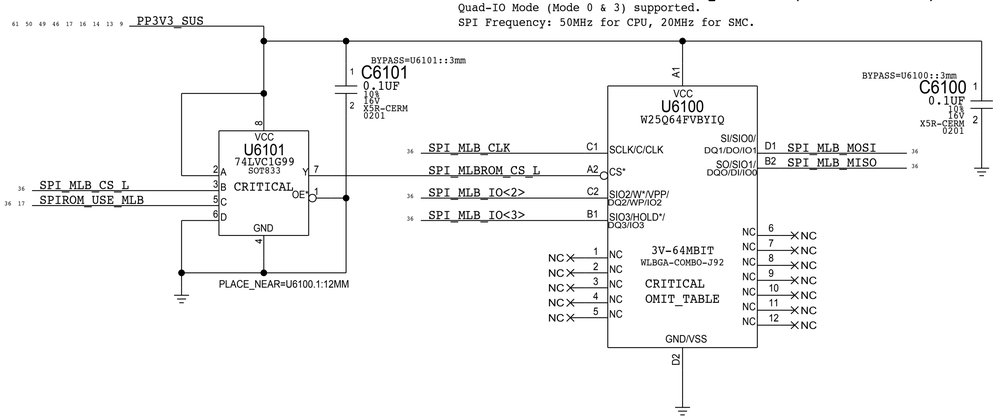
BRANCH: <BRANCH>

PAGE: 55 OF 130

SHEET: 35 OF 67

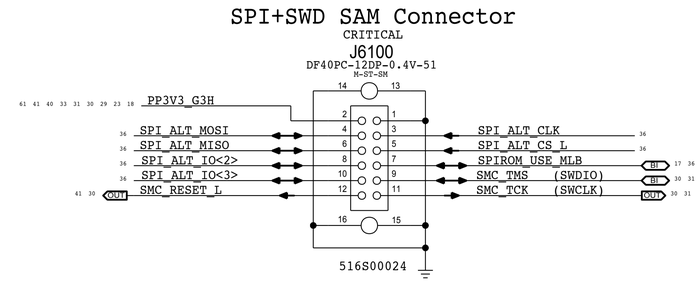
SPI ROM - Combo BGA Footprint (3 vendors)

Quad-IO Mode (Mode 0 & 3) supported.
SPI Frequency: 50MHz for CPU, 20MHz for SMC.



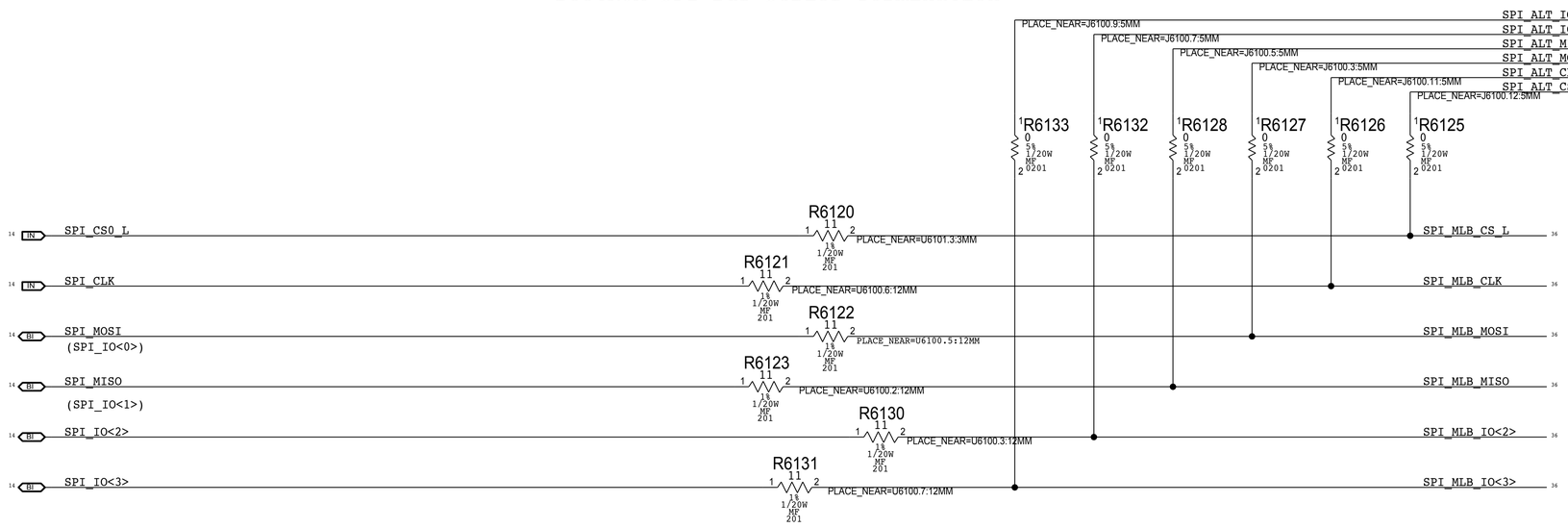
SPI+SWD SAM Connector

CRITICAL



BootROM SPI Bus Series Termination

CPU Master



Sam Card ROM Slave

SPI ROM Slave

SYNC_MASTER=J92_DEVMLB SYNC_DATE=07/23/2013

PAGE TITLE

SPI+SWD Debug Connector

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

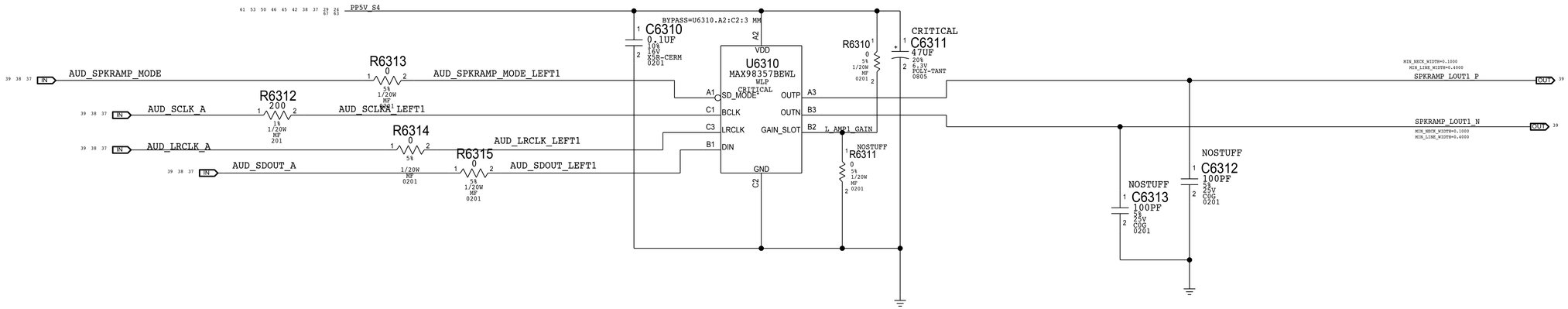
BRANCH <BRANCH>

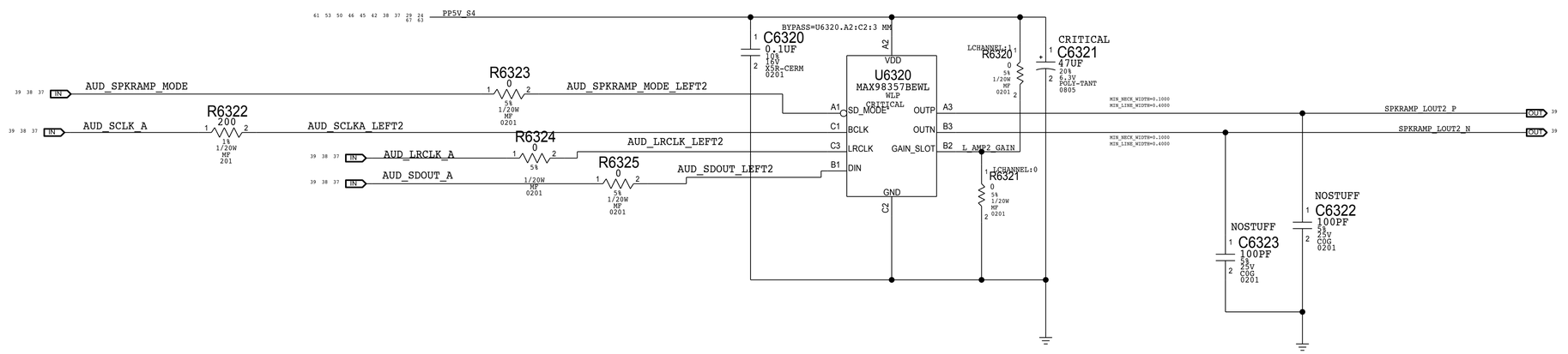
PAGE 61 OF 130

SHEET 36 OF 67

Left Speaker Amps

APPLE P/N 353S4265





SPEAKER CONFIGS

BOM GROUP	BOM OPTIONS
EQ:2CH	LCHANNEL:1,RCHANNEL:3
EQ:4CH	LCHANNEL:0,RCHANNEL:4

SYNC_MASTER=J92_DEVMLB SYNC_DATE=09/19/2013

PAGE TITLE

AUDIO Left Speaker Amps

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

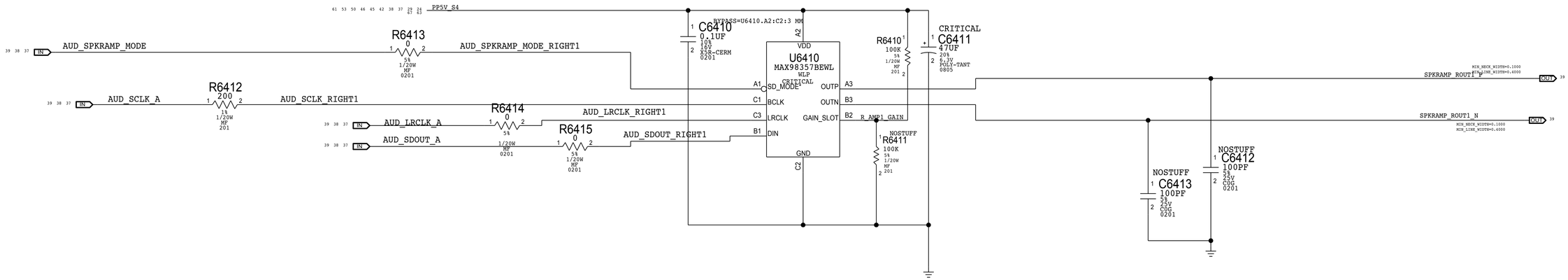
BRANCH <BRANCH>

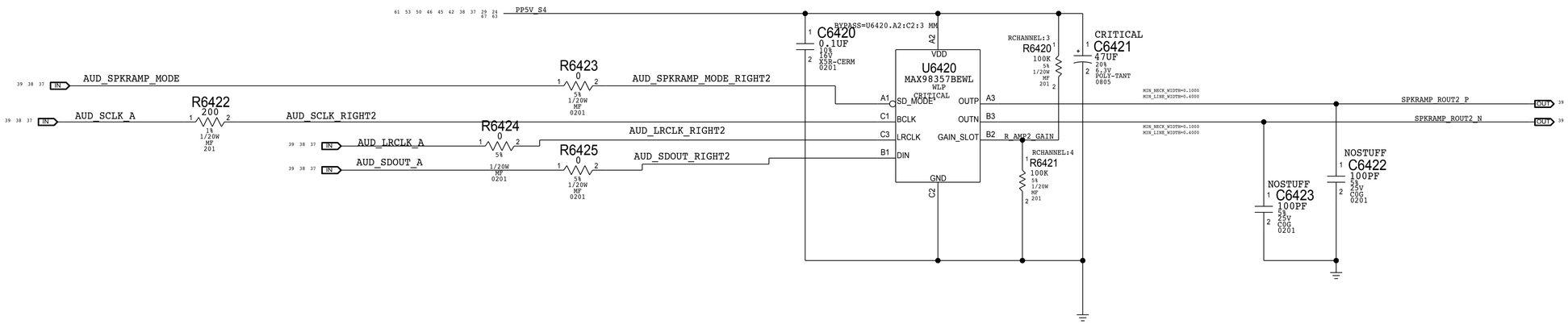
PAGE 63 OF 130

SHEET 37 OF 67

Right Speaker Amps

APPLE P/N 353S4265





SYNC_MASTER=J92_DEVMLB SYNC_DATE=09/19/2013

PAGE TITLE

AUDIO Right Speaker Amps

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 64 OF 130

SHEET 38 OF 67

CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL	DET ASSIGNMENT
HP/LINE OUT	0X02 (2)	0X02 (2)	0X09 (9,A)		0X09 (A)
SPEAKERS	0X04 (4)	0X04 (4)	0X0B (11)	GPIO_3	N/A

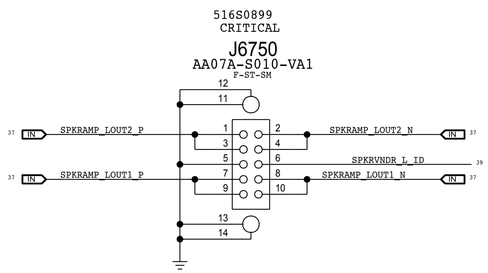
CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	VREF	DET ASSIGNMENT
BUILT-IN MIC	0X06 (6)	0X0D (13,B,RIGHT)	MIC_BIAS (80%)	N/A
HEADSET MIC	0X06 (6)	0X0D (13,V22,B,LEFT)	MIKEY	MIKEY

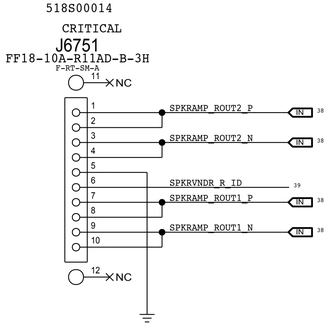
SOUTHBRIDGE RESOURCE/PIN ALLOCATIONS

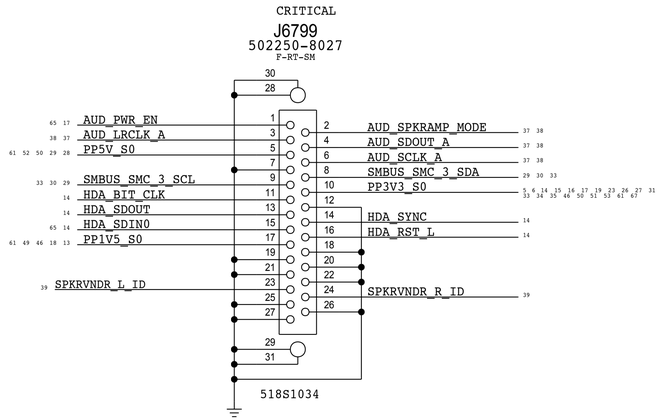
FUNCTION	NET NAME	SB GPIO/INT
PERIPHERAL/EXTRACTION DETECT	AUD_IP_PERIPHERAL_DET	GPIO 3
MIKEY INTERRUPT	AUD_I2C_INT_L	GPIO 5
MIKEY ENABLE	AUD_IPHS_SWITCH_EN	GPIO 16
MIKEY I2C BUS	I2C_MIKEY_SDA/SCL	PCH SMBUS 0

LEFT SPEAKER CONN



RIGHT SPEAKER CONN





RIO FLEX CONN

SYNC_MASTER=CARA_J92 SYNC_DATE=04/17/2014

PAGE TITLE

AUDIO CONNECTORS

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

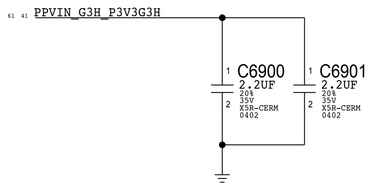
REVISION <E4LABEL>

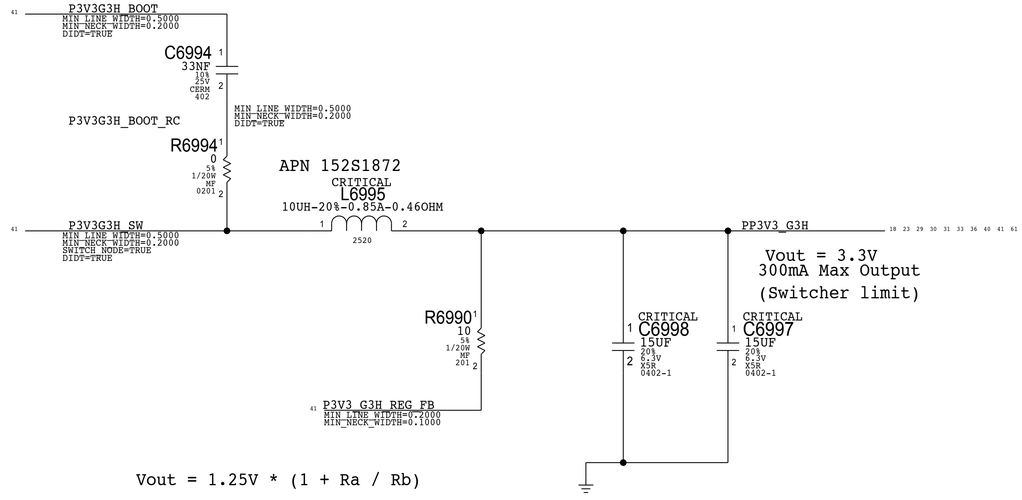
BRANCH <BRANCH>

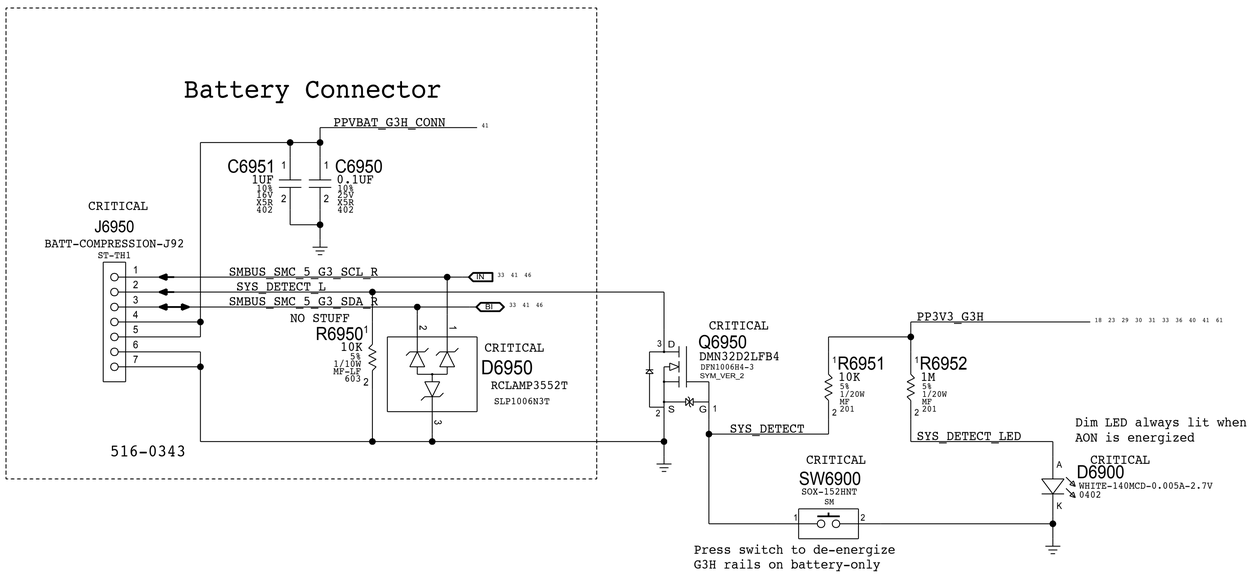
PAGE 67 OF 130

SHEET 39 OF 67

3.3V G3H VR - Bansuri







SYNC_MASTER=(J41_MLB)	SYNC_DATE=03/16/2015
PAGE TITLE	Battery Connector & 3.3V G3Hot
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
	PAGE 69 OF 130
	SHEET 40 OF 67

Charger PMIC - Bansuri

FROM ADAPTER
PPDCIN_G3H
PPVIN_G3H_P3V3G3H
PPVBAT_G3H_CONN
PP3V3_G3H
PP3V3R3V0_AON

U7000
ISL95530HIZ-TR5664
WCSP

R7010 750K 1% 1/20W MF 201
R7011 255K 1% 1/20W MF 201
R7004 4.7 5% 1/20W MF 201
R7001 0 5% 1/20W MF 0201
R7021 5% 1/20W MF 201
R7022 5% 1/20W MF 201
R7020 0.020 OHM 1% 1/3W N/A 0306
R7025 0 5% 1/20W MF 0201
R7027 0 5% 1/20W MF 0201
R7060 100K 5% 1/20W MF 201
R7061 10K 5% 1/20W MF 201
R7050 0.010 OHM 1% 1/3W N/A 0603-COMBO
R7051 5% 1/20W MF 201
R7052 5% 1/20W MF 201

C7004 1UF 10% 25V X5R 0402-1
C7005 1UF 10% 25V X5R 0402-1
C7007 0.1UF 10% 35V CER-X5R 0201
C7000 1UF 10% 25V X5R 0402-1
C7001 1UF 10% 25V X5R 0402-1
C7006 1UF 10% 25V X5R 0402-1
C7020 NOSTUFF 0.047UF 10% 6.3V X5R 201
C7022 1UF 10% 25V X5R 402
C7021 1UF 10% 25V X5R 402
C7025 0.1UF 10% 25V X7R-CERM-1 0402
C7027 0.1UF 10% 25V X7R-CERM-1 0402
C7030 6.8UF 20% 35V-0.150OHM POLY-TANT CASE-B1S
C7031 6.8UF 20% 35V-0.150OHM POLY-TANT CASE-B1S
C7032 6.8UF 20% 35V-0.150OHM POLY-TANT CASE-B1S
C7035 2.2UF 20% 35V X5R-CERM 0402
C7036 2.2UF 20% 35V X5R-CERM 0402
C7037 0.001UF 10% 50V X7R-CERM 0402
C7019 2.2UF 20% 25V X5R-CERM 0402-1
C7016 0.33UF 10% 25V X5R 0402
C7011 0.01UF 10% 10V X5R-CERM 0201
C7050 NOSTUFF 0.047UF 10% 16V X5R 0201
C7018 1000PF 10% 25V X7R-CERM 0201
C7017 2.2UF 20% 25V X5R-CERM 0402-1
C7014 2.2UF 20% 25V X5R-CERM 0402-1
C7013 0.1UF 10% 25V X5R 402
C7012 0.01UF 10% 25V X7R 402
C7002 10UF 20% 10V X5R-CERM 0402-7
C7003 10UF 20% 10V X5R-CERM 0402-7
C7028 0.47UF 10% 25V CER-X5R 0402
C7029 0.47UF 10% 25V CER-X5R 0402
C7026 4700PF 10% 25V CER-X5R 0201
C7043 33UF 20% 16V TANT CASE-B1S
C7047 33UF 20% 16V TANT CASE-B1S
C7044 2.2UF 20% 25V X5R-CERM 0402-1
C7046 2.2UF 20% 25V X5R-CERM 0402-1
C7045 1000PF 10% 16V X7R-1 0201
C7010 0.1UF 10% 16V X5R-CERM 0201

L7030 APN 152S00224 CRITICAL 2UH-20%-9.3A-0.024OHM PIME062T

Q7010 APN 376S1203 CRITICAL SIZ342JT PWRPAIR-3X3
Q7020 CRITICAL CSD58879Q3D Q3D APN 376S1187
Q7055 CRITICAL SI7655DN PWRPK-1212-8 APN 376S1179

F7040 CRITICAL 8AMP-32V-0.0060HM 0603

NOSTUFF C7020 0.047UF 10% 6.3V X5R 201

P_IN CRITICAL
ACIN
SDA
SCL
GPIO1
GATE_Q1
GATE_Q2
GATE_Q3
GATE_Q4
POWER_GATE_EN
BGATE
COMP
CSIN
CSIP
HPWR_EN
CSON
BMON
SMC_RST_IN
SMC_RST*
PBUS
PBUS
LX1
LX2
LX_VR1
LX_VR2
LX_VR2
BOOT1
BOOT2
BOOT_VR1
BOOT_VR2
EN_VR2
PGOOD_VR2
FB_VR1
FB_VR2
LDO_3P0
LDO_5P0
AMON
ACOK
HOST_RESET
CSOP
CBC_ON
IRQ_L
AGND
AGND
AGND
PGND
PGND_VR2
PGND_VR2
PGND_VR1

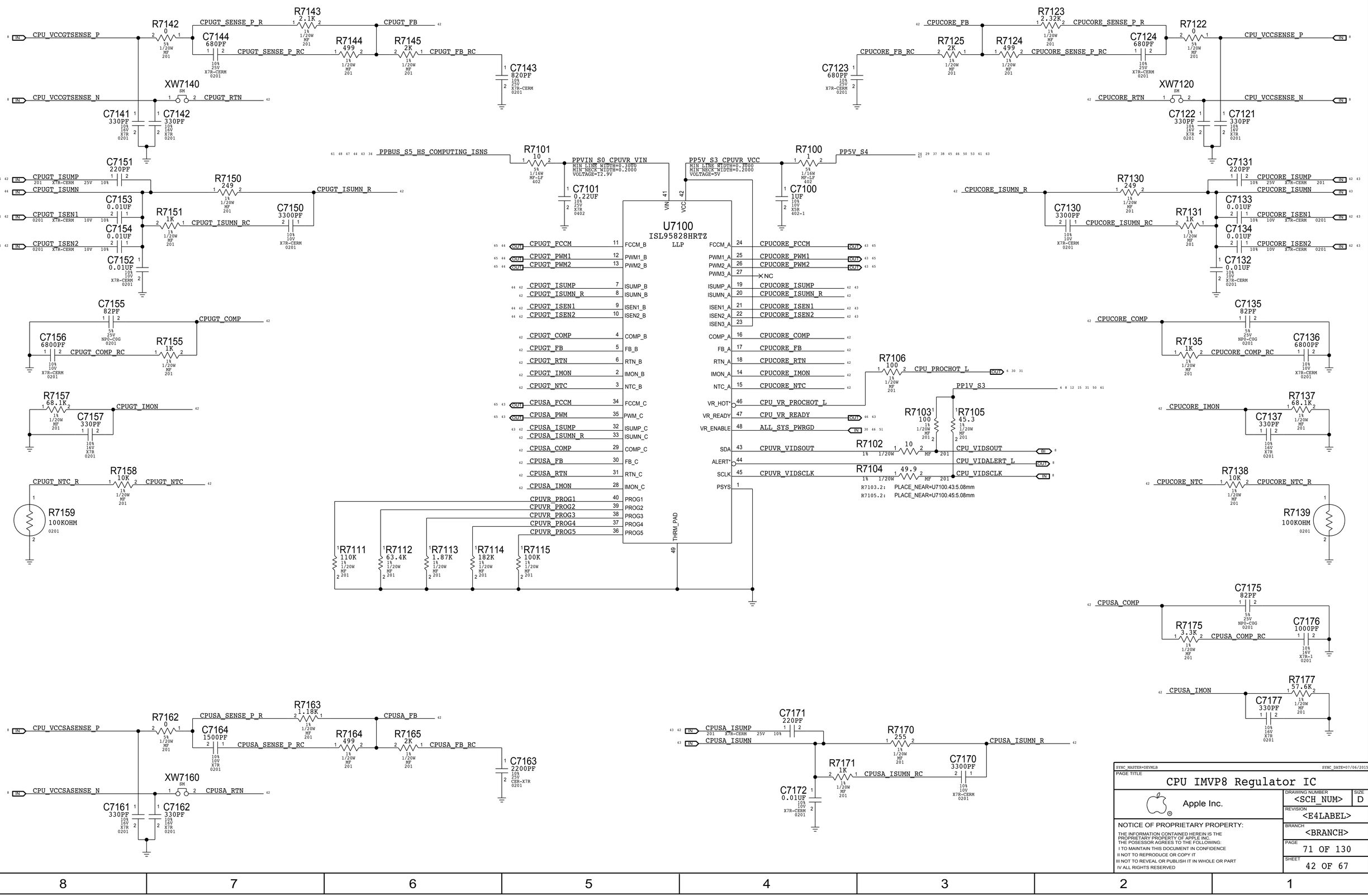
CHGR_PHASE
CHGR_BOOST_SW
P3V3G3H_SW
CHGR_BOOT1_RC
CHGR_BOOT1
CHGR_BOOT2
CHGR_BOOT2_RC
P3V3G3H_BOOT
P3V3_G3H_REG_FB
CHGR_LDO_P3V0
CHGR_LDO_P5V0
CHGR_AMON
SMC_BC_ACOK
TS_HOST_RST
CHGR_CSO_P
SMC_CBC_ON
SMC_CHGR_INT_L

CHGR_ACIN
SMBUS_SMC_5_G3_SDA_R
SMBUS_SMC_5_G3_SCL_R
CHGR_BUCK_DH
CHGR_BUCK_DL
CHGR_BOOST_DL
CHGR_BOOST_DH
POWER_GATE_EN
CHGR_BGATE
CHGR_COMP
CHGR_CSI_N
CHGR_CSI_P
HIPWR_EN
CHGR_CSO_N
CHGR_BMON
SMC_LSOC_RST
SMC_RST_L
SMC_RESET_L
PPBUS_G3H

CHGR_LDO_VDDA
CHGR_LDO_VDDP
CHGR_LDO_P5V0
CHGR_CSI_P
CHGR_CSI_N
CHGR_CSI_R_P
CHGR_CSI_R_N
PPDCIN_G3H_CHGR
PPVBAT_G3H_CHGR_REG
PPVBAT_G3H_CHGR_R
PPVBAT_G3H_CONN
PPBUS_G3H
TO SYSTEM
TO/FROM BATTERY
CHGR_CSO_R_P
CHGR_CSO_R_N
(CHGR_CSO_P)
(CHGR_CSO_N)
(CHGR_BGATE)
(CHGR_PHASE)
CHGR_BOOST_DH
CHGR_BOOST_SW
CHGR_BOOST_DL

BYPASS=Q7010.2::1.5mm

SYNC_MASTER=DEVMLB	SYNC_DATE=05/11/2015
PAGE TITLE: PBus Supply & Battery Charger	
Apple Inc.	DRAWING NUMBER: <SCH_NUM> SIZE: D
	REVISION: <E4LABEL>
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED	BRANCH: <BRANCH> PAGE: 70 OF 130 SHEET: 41 OF 67



SYNC_MASTER=DEVNLB SYNC_DATE=07/06/2015

PAGE TITLE

CPU IMVP8 Regulator IC

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 71 OF 130

SHEET 42 OF 67

Note:Vcore design requires 4x POSCAPs
3x shared from other VRs

CPU VCORE

Phase 1

PPBUS_S5_HS_COMPUTING_ISNS

CRITICAL C7210 33UF 20% 16V TANT CASE-B1S
CRITICAL C7211 33UF 20% 16V TANT CASE-B1S
C7214 2.2UF 20% 25V X6S-CERM 0402
C7215 2.2UF 20% 25V X6S-CERM 0402

PP5V_S0_CPUCORE1
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.2000
VOLTAGE=5V

R7217 2.2 1% 1/20W MF 201
C7217 2.2UF 20% 25V X6S-CERM 0402
C7216 2.2UF 20% 25V X6S-CERM 0402

PP5V_S4RS0

CPUCORE_BOOT1_R
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.2000
DIDT=TRUE

R7219 0 5% 1/16W MF-LF 402
C7219 0.22UF 10% 25V X7R 0402

U7210
SIC535CD
MLP4535

	VIN	BOOT	CPUCORE_BOOT1 (MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.2000, DIDT=TRUE)
CPUCORE_FCCM (IN 65 43 42)	ZCD_EN*	PHASE	CPUCORE_BOOT1_RC (MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.2000, DIDT=TRUE)
CPUCORE_PWM1 (IN 65 42)	PWM	VSWH	CPUCORE_PHASE1 (MIN_LINE_WIDTH=0.6000, MIN_NECK_WIDTH=0.2000, DIDT=TRUE, SWITCH_NODE=TRUE)
NC	NC	GL	CPUCORE_GL1 (65)
		GL	NC
	PGND		
	PGND		
	CGND		

XW7210 SM

GND_CPUCORE1_CGND
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.2000
VOLTAGE=0V

CRITICAL L7210 0.22UH-20%-12A-0.0045OHM PILE052T-SM 152S00217
PPVCORE_S0_CPU_PH1
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2000
VOLTAGE=1.5V

CRITICAL R7210 0.001 1% 1/2W MF 0306

CPUCORE_ISNS1_P (OUT 64)
CPUCORE_ISNS1_N (OUT 43 64)
NO_XNET_CONNECTION=1
R7214 2.2 1% 1/20W MF 201
CPUCORE_ISUMN (OUT 62 43)

NO_XNET_CONNECTION=1
R7211 1K 1% 1/20W MF 201
NO_XNET_CONNECTION=1
R7212 200K 1% 1/20W MF 201
R7213 200K 1% 1/20W MF 201
CPUCORE_ISNS2_N (43 64)
NO_XNET_CONNECTION=1
CPUCORE_ISEN1 (OUT 62)
CPUCORE_ISUMP (OUT 62 43)

PPVCORE_S0_CPU (8 11 34 61)

Vout = 1.50V max
24A max load
f = 750kHz

Phase 2

PPBUS_S5_HS_COMPUTING_ISNS

CRITICAL C7230 33UF 20% 16V TANT CASE-B1S
CRITICAL C7231 33UF 20% 16V TANT CASE-B1S
C7234 2.2UF 20% 25V X6S-CERM 0402
C7235 2.2UF 20% 25V X6S-CERM 0402

PP5V_S0_CPUCORE2
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.2000
VOLTAGE=5V

R7237 2.2 1% 1/20W MF 201
C7237 2.2UF 20% 25V X6S-CERM 0402
C7236 2.2UF 20% 25V X6S-CERM 0402

PP5V_S4RS0

CPUCORE_BOOT2_R
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.2000
DIDT=TRUE

R7239 0 5% 1/16W MF-LF 402
C7239 0.22UF 10% 25V X7R 0402

U7230
SIC535CD
MLP4535

	VIN	BOOT	CPUCORE_BOOT2 (MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.2000, DIDT=TRUE)
CPUCORE_FCCM (IN 65 43 42)	ZCD_EN*	PHASE	CPUCORE_BOOT2_RC (MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.2000, DIDT=TRUE)
CPUCORE_PWM2 (IN 65 42)	PWM	VSWH	CPUCORE_PHASE2 (MIN_LINE_WIDTH=0.6000, MIN_NECK_WIDTH=0.2000, DIDT=TRUE, SWITCH_NODE=TRUE)
NC	NC	GL	CPUCORE_GL2 (65)
		GL	NC
	PGND		
	PGND		
	CGND		

XW7230 SM

GND_CPUCORE2_CGND
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.2000
VOLTAGE=0V

CRITICAL L7230 0.22UH-20%-12A-0.0045OHM PILE052T-SM 152S00217
PPVCORE_S0_CPU_PH2
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2000
VOLTAGE=1.5V

CRITICAL R7230 0.001 1% 1/2W MF 0306

CPUCORE_ISNS2_P (OUT 64)
CPUCORE_ISNS2_N (OUT 43 64)
NO_XNET_CONNECTION=1
R7234 2.2 1% 1/20W MF 201
CPUCORE_ISUMN (OUT 62 43)

NO_XNET_CONNECTION=1
R7231 1K 1% 1/20W MF 201
NO_XNET_CONNECTION=1
R7232 200K 1% 1/20W MF 201
R7233 200K 1% 1/20W MF 201
CPUCORE_ISNS1_N (43 64)
NO_XNET_CONNECTION=1
CPUCORE_ISEN2 (OUT 62)
CPUCORE_ISUMP (OUT 62 43)

CPU VCCSA

PP5V_S4RS0

C7290 33UF 20% 16V TANT CASE-B1S
C7294 2.2UF 20% 25V X6S-CERM 0402
C7295 2.2UF 20% 25V X6S-CERM 0402

CPUSA_BOOT_R
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.2000
DIDT=TRUE

C7296 2.2UF 20% 25V X6S-CERM 0402
R7299 0 5% 1/16W MF-LF 402
C7299 0.22UF 10% 25V X7R 0402

U7290
ISL6208D
DFN
CRITICAL

CPUSA_PWM (IN 65 42)	PWM	BOOT	CPUSA_BOOT (MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.2000, DIDT=TRUE)
CPUSA_FCCM (IN 65 42)	FCCM	UGATE	CPUSA_UGATE (MIN_LINE_WIDTH=0.4000, MIN_NECK_WIDTH=0.2000, DIDT=TRUE, GATE_NODE=TRUE)
		PHASE	CPUSA_PHASE (MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.2000, DIDT=TRUE, SWITCH_NODE=TRUE)
		LGATE	CPUSA_LGATE (MIN_LINE_WIDTH=0.4000, MIN_NECK_WIDTH=0.2000, DIDT=TRUE, GATE_NODE=TRUE)
	VCC		
	GND		
	THRM PAD		

CRITICAL Q7291 CSD58873Q3D Q3D

VIN	1
TG	3
TGR	4
VSW	6, 7, 8
BG	5
PGND	9

CPUSA_SW_LL
MIN_LINE_WIDTH=0.4000
MIN_NECK_WIDTH=0.2000
DIDT=TRUE
SWITCH_NODE=TRUE

CRITICAL L7290 0.47UH-20%-8.5A-0.0035OHM PIMA032T-SM
PPVCCSA_S0_CPU
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2000
VOLTAGE=1.5V

CRITICAL R7290 0.003 1% 1/2W MF 0306

CPUSA_ISNS_P (OUT 64)
CPUSA_ISNS_N (OUT 64)

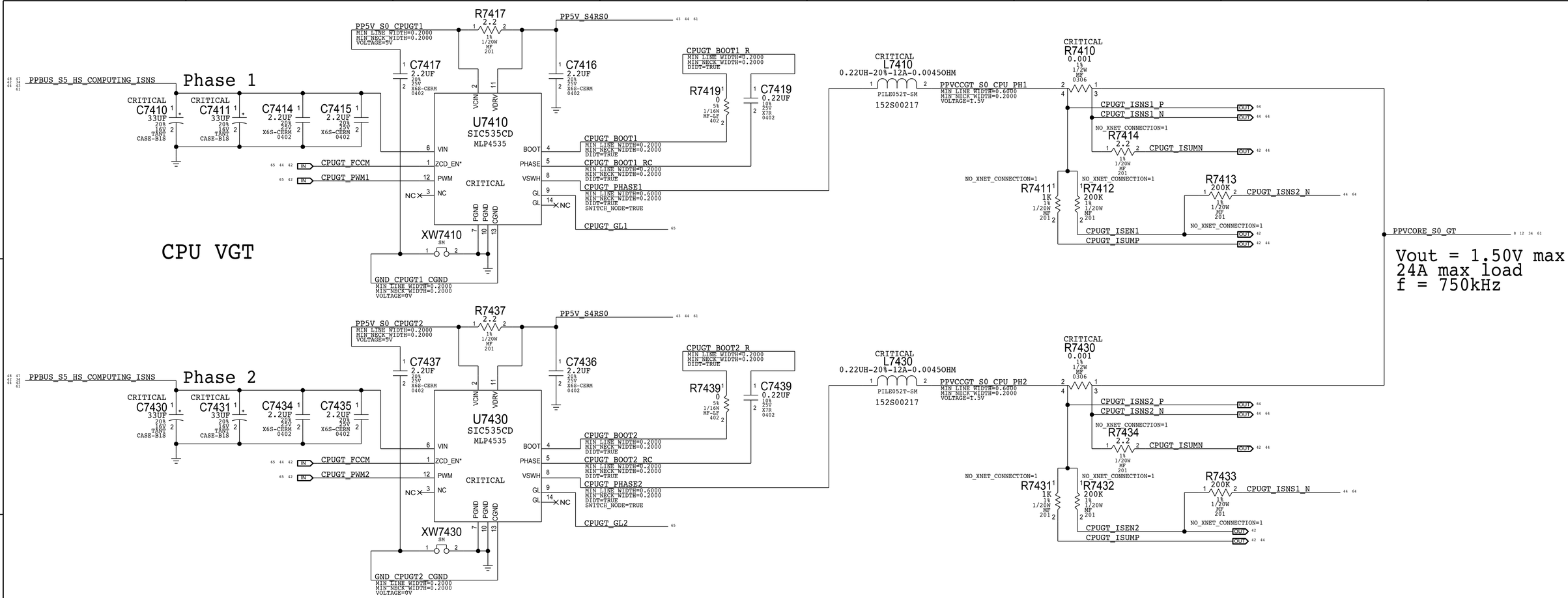
XW7290 SM
PLACE_NEAR=R7290:5MM
PPVCCSA_DDR_S0 (0 11 61)
PPVCCSA_S0 (0 11 61)

Vout = 1.05V max
4.1A max load
f = 750kHz

NO_XNET_CONNECTION=1
R7291 1K 1% 1/20W MF 201
NO_XNET_CONNECTION=1
R7292 0 5% 1/20W MF 0201
CPUSA_ISUMN (OUT 42)
CPUSA_ISUMP (OUT 42)

SYNC_MASTER=DEVMLB	SYNC_DATE=05/19/2015
PAGE TITLE	CPU VCore/VccSA Power Stage
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
	PAGE 72 OF 130
	SHEET 43 OF 67

CPU & CHIPS



SYNC_MASTER=DEVMLB SYNC_DATE=05/11/2015

PAGE TITLE

CPU VccGT Power Stage

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 74 OF 130

SHEET 44 OF 67

5.1V S4

3.3V S5 (DSW)

PPBUS_G3H

PP5V_S4

PP5V_S5

PP3V3_S5

VOUT = 5.1V
7.3 A MAX OUTPUT
F = 400 KHZ

VOUT = 5V
CRITICAL100MA MAX OUTPUT

VOUT = 3.3V
4.2 A MAX OUTPUT
F = 400 KHZ

CRITICAL U7650 TPS51980A QFN

CRITICAL Q7660 FDPC1012S LLP

CRITICAL Q7680 CSD58873Q3D Q3D

CRITICAL L7670 1.5UH-20%-13A-0.0265OHM PIMS062T-SM

CRITICAL L7690 1.8UH-20%-8.5A-0.0325OHM PIMA052T-SM

P5VS4_TG
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2000
GATE_NODE=TRUE
DIDT=TRUE

P5VS4_VBST_R
MIN_LINE_WIDTH=0.0950
MIN_NECK_WIDTH=0.0700
SWITCH_NODE=TRUE

P5VP3V3_VREG3

P5VP3V3_VREF2

P3V3S5_TG
MIN_LINE_WIDTH=0.0950
MIN_NECK_WIDTH=0.0700
DIDT=TRUE
GATE_NODE=TRUE

P3V3S5_VBST_R
MIN_LINE_WIDTH=0.0950
MIN_NECK_WIDTH=0.0700
SWITCH_NODE=TRUE

P5VS4_VBST
P5VS4_DRVH
P5VS4_VSW
P5VS4_DRVL
P5VS4_CSP1
P5VS4_CSN1
P5VS4_VFB1
P5VS4_COMP1
PM_SLP_S5_L
P5VS4_PGOOD
S5_PWR_EN
S5_PWRGD
P3V3S5_VBST
P3V3S5_DRVH
P3V3S5_SW2
P3V3S5_DRVL
P3V3S5_CSP2
P3V3S5_CSN2
P3V3S5_RF
P3V3S5_VFB2
P3V3S5_COMP2
P3V3S5_VSW

P5VS4_VFB1_R
P5VS4_VFB1_RR
P5VS4_CSP1_R
P5VS4_COMP1_R
P3V3S5_COMP2_R
P3V3S5_CSP2_R
P3V3S5_VFB2_R
P3V3S5_VFB2_RR

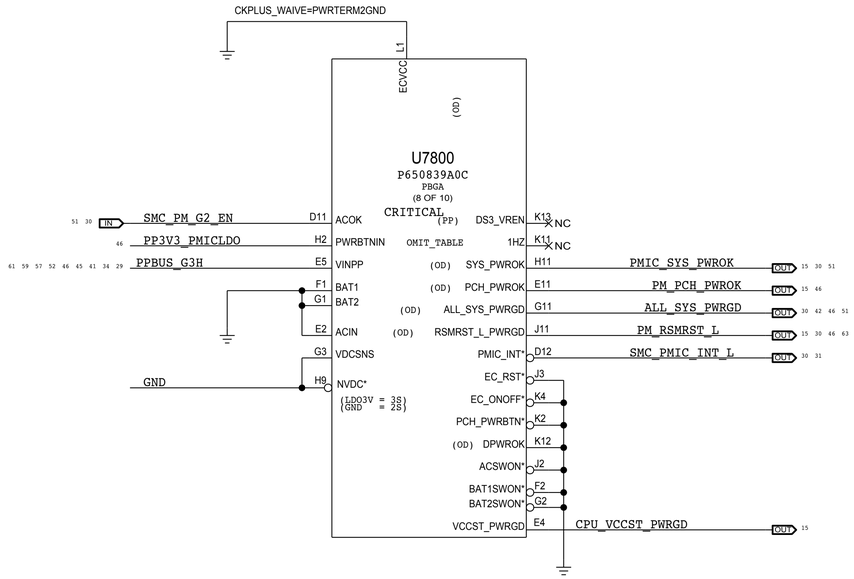
PLACE_NEAR=U7650.28:1MM

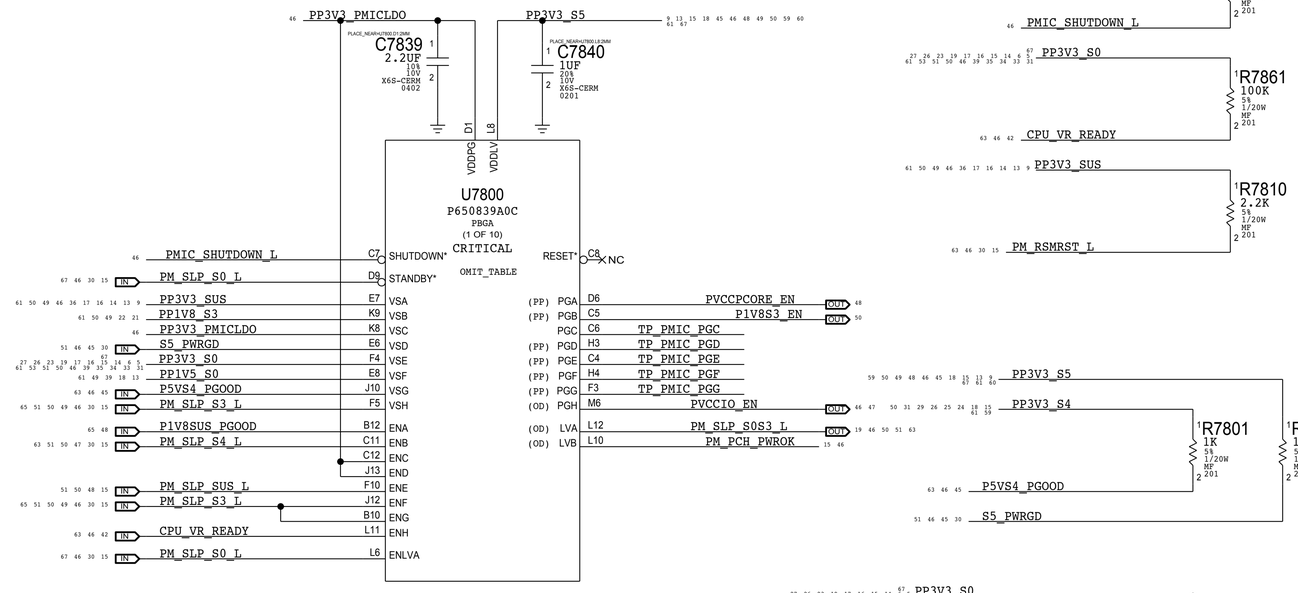
GND_5V3V3_AGND
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.2000
VOLTAGE=0V

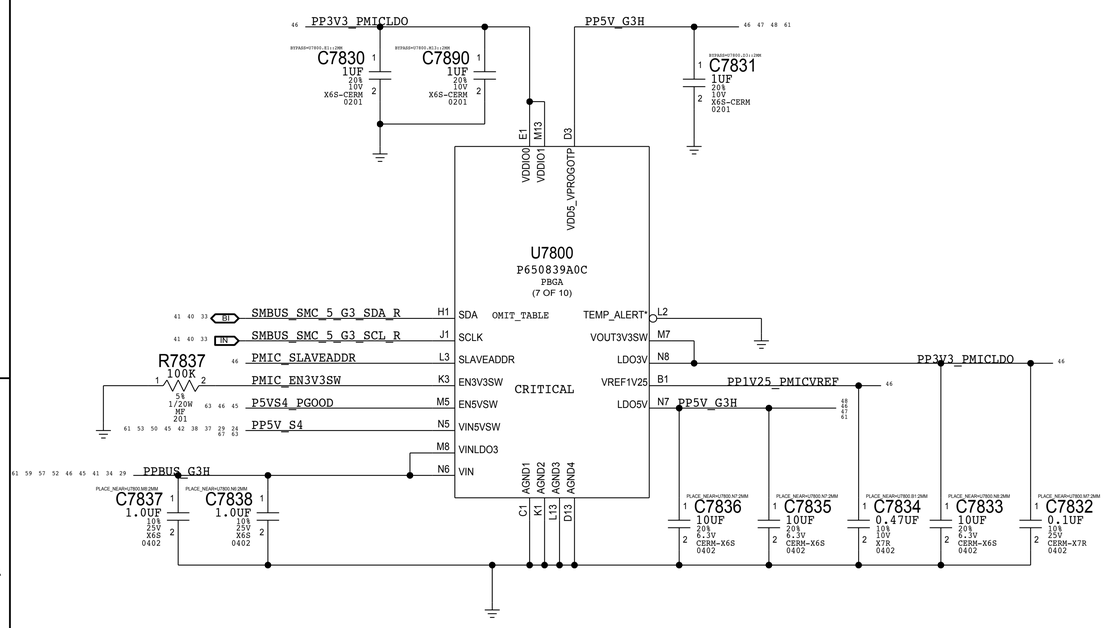
NO STUFF

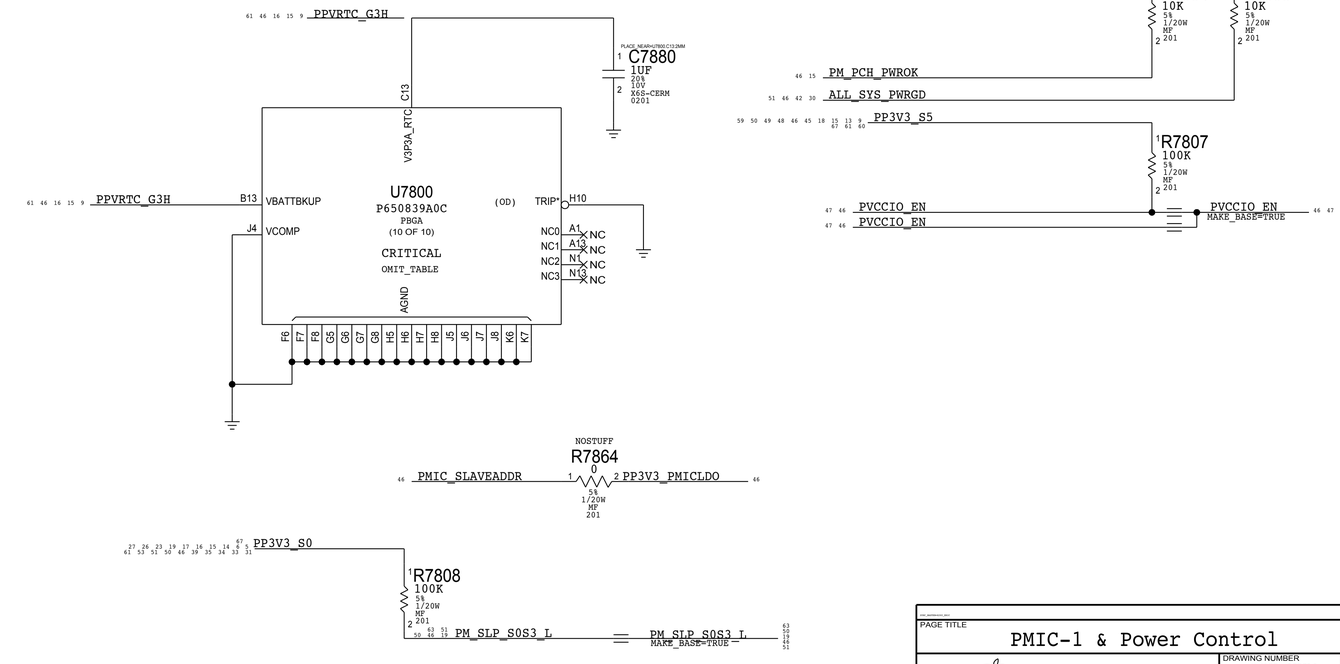
SYNC_MASTER=J92_MLB	SYNC_DATE=03/20/2015
PAGE TITLE: 5V & 3.3V Power Supplies	
Apple Inc.	DRAWING NUMBER: <SCH_NUM> SIZE: D
	REVISION: <E4LABEL>
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED	BRANCH: <BRANCH> PAGE: 76 OF 130 SHEET: 45 OF 67

BANJO - PMIC Control









PAGE TITLE

PMIC-1 & Power Control

Apple Inc.

DRAWING NUMBER <SCH_NUM> | SIZE D

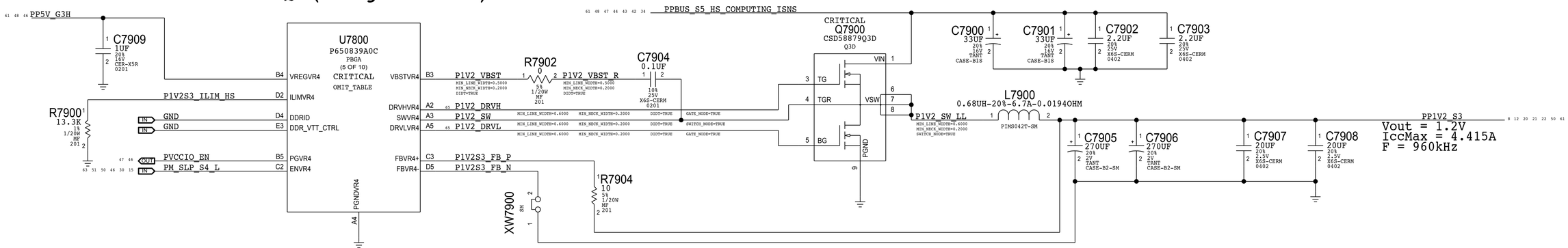
REVISION <E4LABEL>

BRANCH <BRANCH>

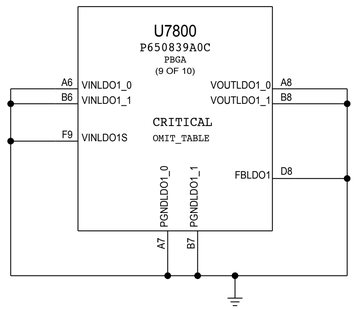
PAGE 78 OF 130

SHEET 46 OF 67

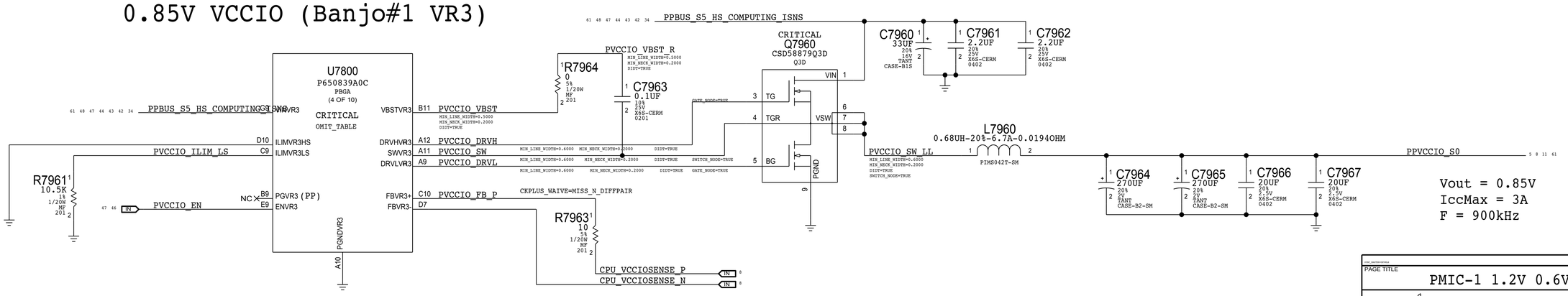
1.2V VDDQ (Banjo#1 VR4)



0.6V VTT (Banjo#1 LDO1)



0.85V VCCIO (Banjo#1 VR3)



PAGE TITLE

PMIC-1 1.2V 0.6V VCCIO

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

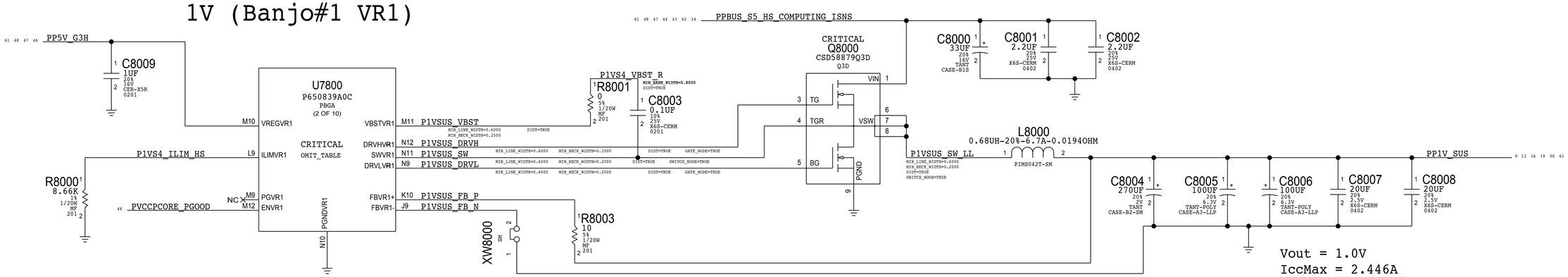
REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 79 OF 130

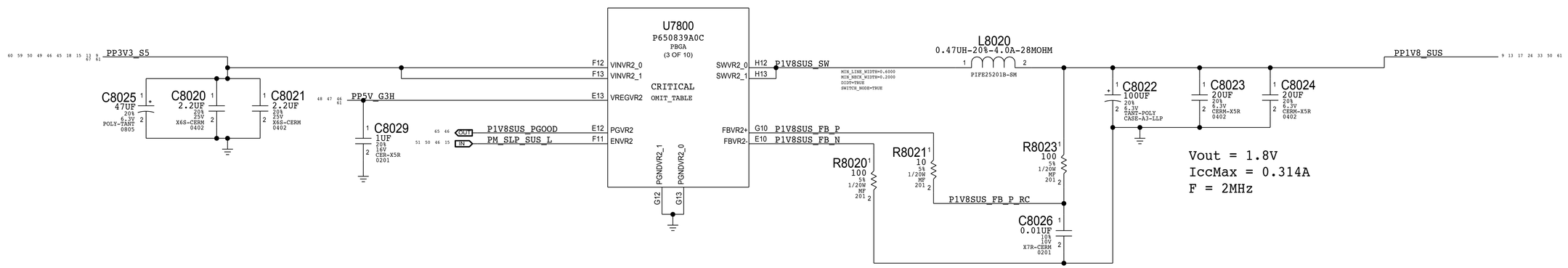
SHEET 47 OF 67

1V (Banjo#1 VR1)



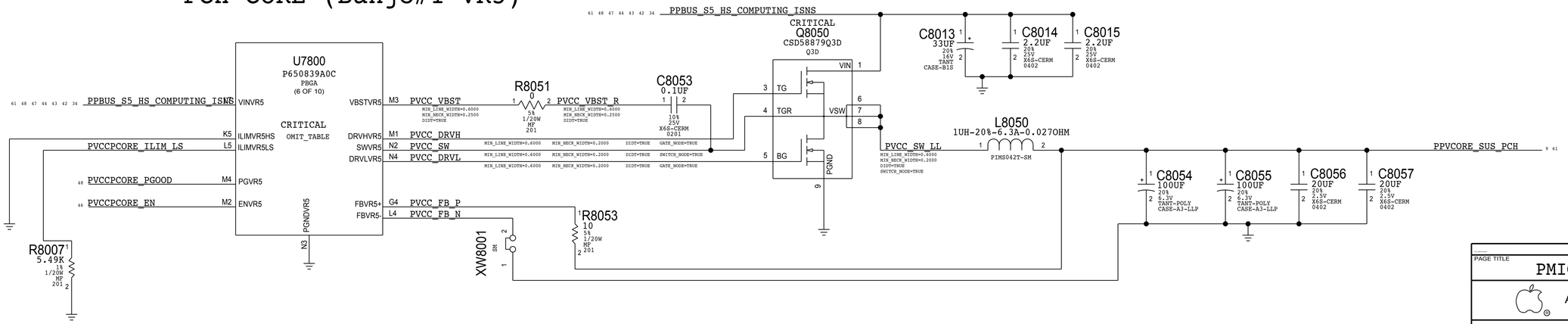
Vout = 1.0V
IccMax = 2.446A
F = 800kHz

1.8V (Banjo#1 VR2)



Vout = 1.8V
IccMax = 0.314A
F = 2MHz

PCH CORE (Banjo#1 VR5)



Vout = Based on VID
IccMax = 1.1A
F = 800kHz

PAGE TITLE

PMIC-1 1V 1.8V VCCPCH

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

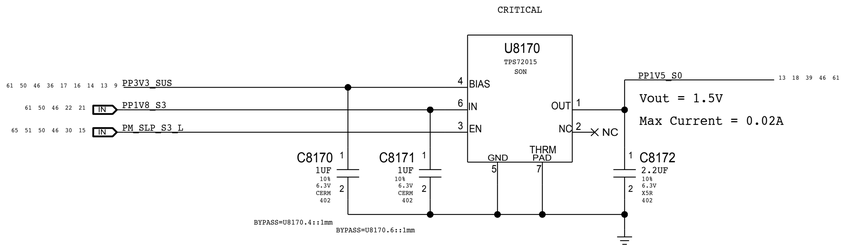
REVISION <E4LABEL>

BRANCH <BRANCH>

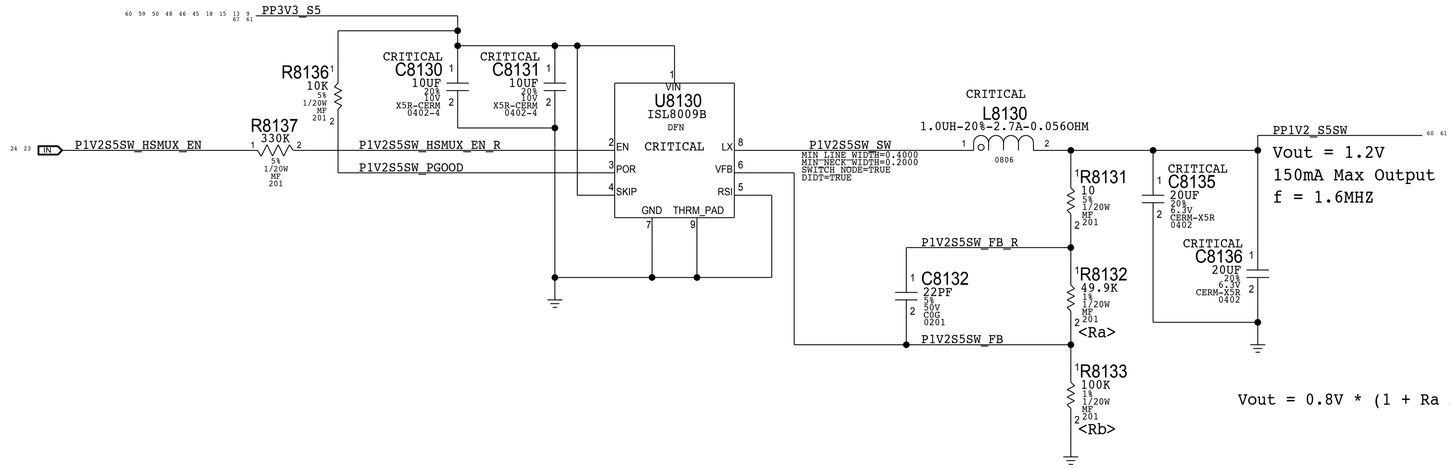
PAGE 80 OF 130

SHEET 48 OF 67

1.5V S0 LDO



1.2V S5 USB-C HS Mux



SYNC_MASTER=X260_ERIC SYNC_DATE=06/15/2015

PAGE TITLE

Misc Power Supplies

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

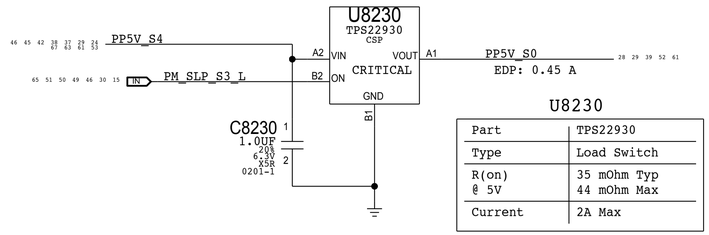
REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 81 OF 130

SHEET 49 OF 67

5V S0 Switch

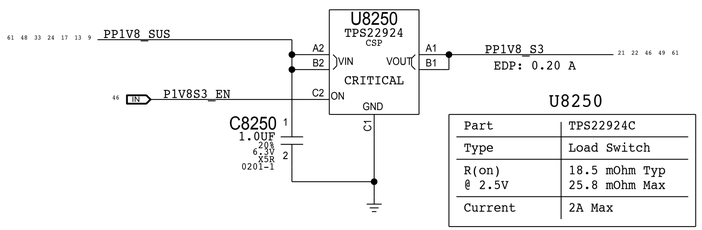


U8230

Part	TPS22930
Type	Load Switch
R(on) @ 5V	35 mOhm Typ 44 mOhm Max
Current	2A Max

1.8V S3 Switch

(LPDDR3)

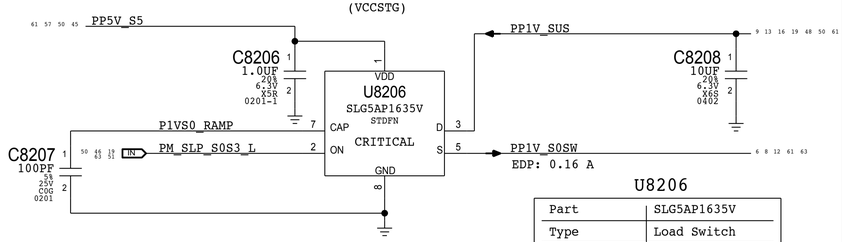


U8250

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max
Current	2A Max

1.0V S0SW Switch

(VCCSTG)

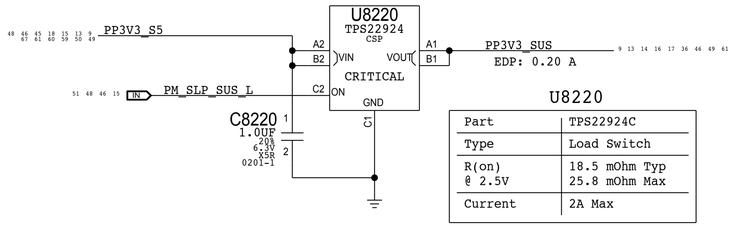


U8206

Part	SLG5AP1635V
Type	Load Switch
R(on) @ 4V Vgs	20 mOhm Typ 28 mOhm Max
Current	2.5A Max

HSIO FET de-featured from SKL
leaving placeholder for CNL

3.3V SUS Switch

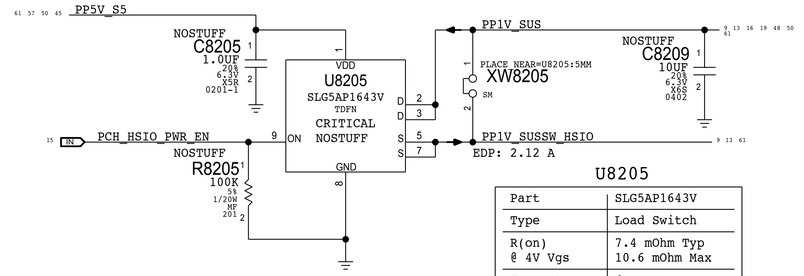


U8220

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max
Current	2A Max

1.0V SUSSW HSIO Switch

(VCCGATED)

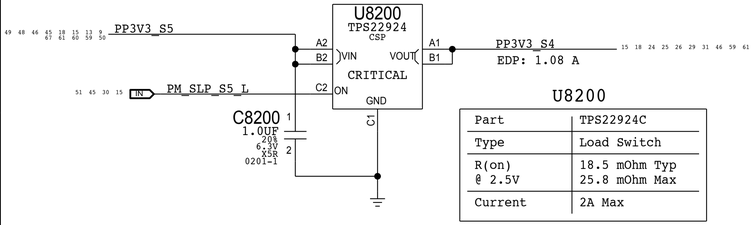


U8205

Part	SLG5AP1643V
Type	Load Switch
R(on) @ 4V Vgs	7.4 mOhm Typ 10.6 mOhm Max
Current	6A Max

HSIO has turn-on requirement of
10uS min and 200uS max
from EN to 0.95V

3.3V S4 Switch

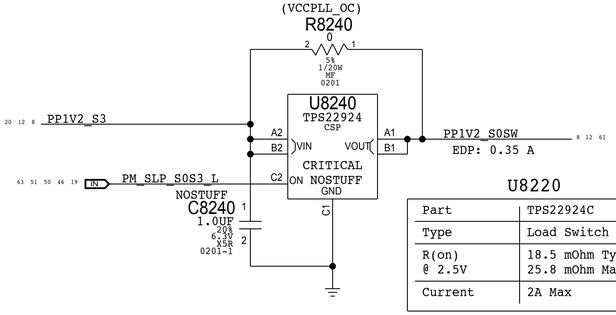


U8200

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max
Current	2A Max

1.2V S0SW Switch

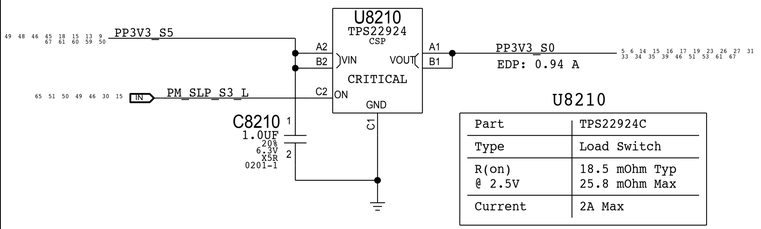
(VCCPLL_OC)



U8220

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max
Current	2A Max

3.3V S0 Switch

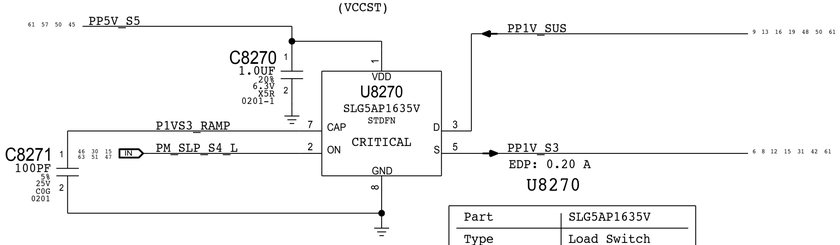


U8210

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max
Current	2A Max

1.0V S3 Switch

(VCCST)



U8270

Part	SLG5AP1635V
Type	Load Switch
R(on) @ 4V Vgs	20 mOhm Typ 28 mOhm Max
Current	2.5A Max

SYNC_MASTER=DEVMLB SYNC_DATE=05/06/2015

PAGE TITLE

Power FETs

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 82 OF 130

SHEET 50 OF 67

Mobile System Power State Table

State	SMC_ADAPTER_EN	SMC_PM_G2_ENABLE	PM_SUS_EN	PM_SLP_S5_L	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	X	1	1	1	1	1
Sleep (S3AC)	1	1	1	1	1	0
Sleep (S3)	0	1	1	1	1	0
Deep Sleep (S4)	0	1	0	1	0	0
Deep Sleep (S5)	0	1	0	0	0	0
Battery Off (G3HotAC)	toggle 3Hz	0	0	0	0	0
Battery Off (G3Hot)	1	0	0	0	0	0

S5 Power Good (3.3V DSW PGOOD based)

51 46 45 30 IN S5_PWRGD — S5_PWRGD MAKE_BASE=TRUE — OUT 30 45 46 51

51 46 30 15 PMIC_SYS_PWROK MAKE_BASE=TRUE — PMIC_SYS_PWROK 15 30 46 51

27 26 23 19 17 16 15 14 6 5
67 61 53 50 46 39 35 34 33 31 PP3V3_S0

R8303 1K 5% 1/20W MF 201 (1 / 2)

51 46 30 15 PMIC_SYS_PWROK

S5 Enables

46 30 IN SMC_PM_G2_EN — D8300 0201 (A / K) RB521ES-30

59 IN STORAGE_LATCH — D8301 0201 (A / K) RB521ES-30

R8300 47K 5% 1/20W MF 201 (1 / 2)

S5_PWR_EN MAKE_BASE=TRUE 45 51

S5_PWR_EN — OUT 45 51

S5_PWR_EN — OUT 45 51

SUS & S4 Enables

51 50 45 30 15 IN PM_SLP_S5_L MAKE_BASE=TRUE — PM_SLP_S5_L — OUT 15 30 45 50 51

PM_SLP_S5_L — OUT 15 30 45 50 51

51 50 48 46 15 IN PM_SLP_SUS_L MAKE_BASE=TRUE — PM_SLP_SUS_L — OUT 15 46 48 50 51

PM_SLP_SUS_L — OUT 15 46 48 50 51

S3 Enables

63 51 50 47 46 30 15 IN PM_SLP_S4_L MAKE_BASE=TRUE — PM_SLP_S4_L — OUT 15 30 46 47 50 51 63

S0 Enables

65 51 50 49 46 30 15 IN PM_SLP_S3_L MAKE_BASE=TRUE — PM_SLP_S3_L — OUT 15 30 46 49 50 51 65

PM_SLP_S3_L — OUT 15 30 46 49 50 51 65

PM_SLP_S3_L — OUT 15 30 46 49 50 51 65

S0I Enables

63 51 50 46 19 IN PM_SLP_S0S3_L MAKE_BASE=TRUE — PM_SLP_S0S3_L — OUT 19 46 50 51 63

51 46 42 30 IN ALL_SYS_PWRGD MAKE_BASE=TRUE — ALL_SYS_PWRGD — OUT 30 42 46 51

$SYNC_MASTER=DEVEL0 $SYNC_DATE=05/11/2015

PAGE TITLE

Power Control

Apple Inc.

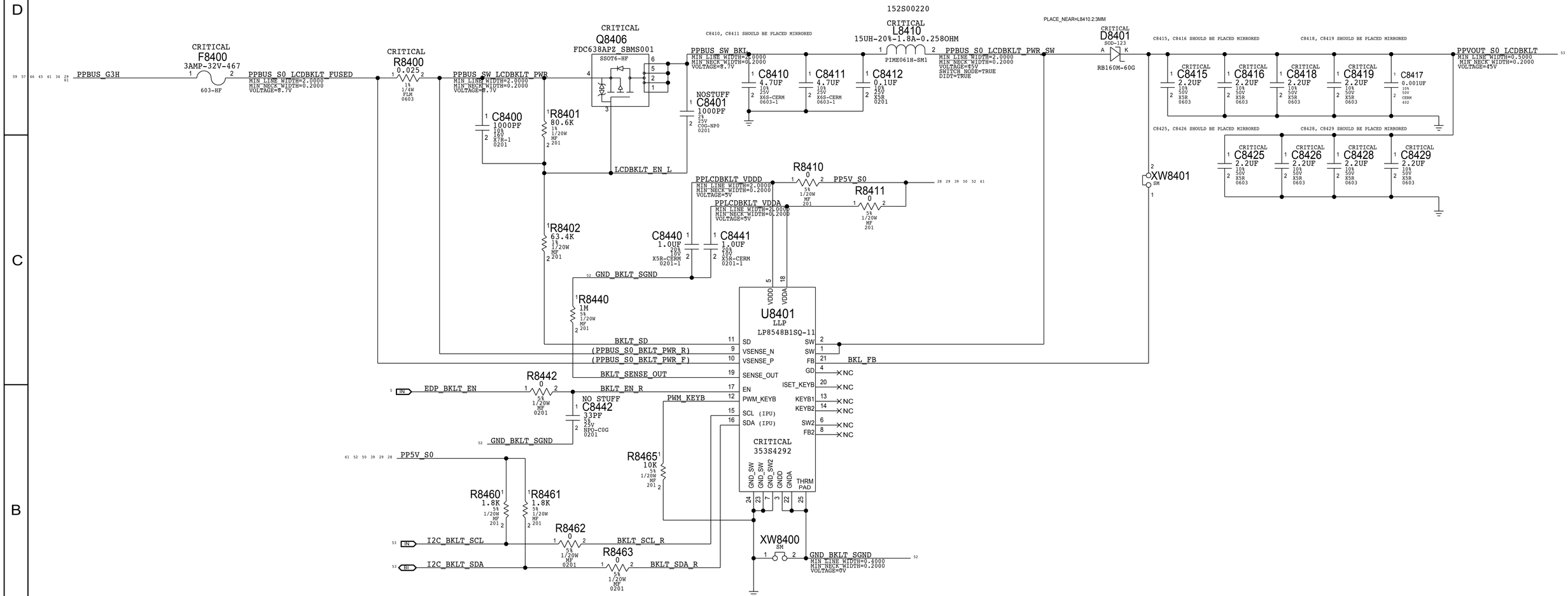
DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 83 OF 130

SHEET 51 OF 67



SYNC_MASTER=DEVMLB SYNC_DATE=03/16/2015

PAGE TITLE

LCD Backlight Driver

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

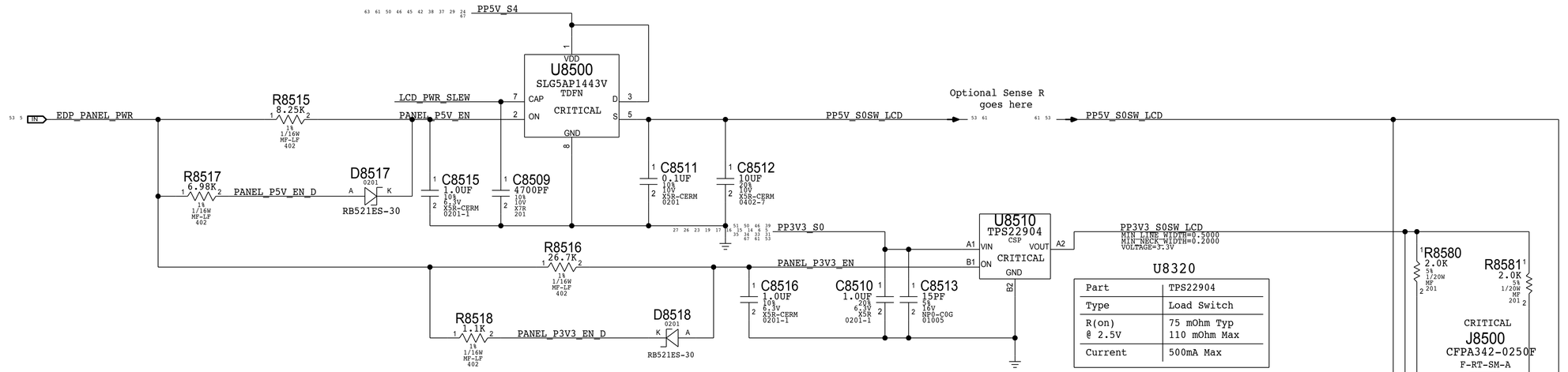
REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 84 OF 130

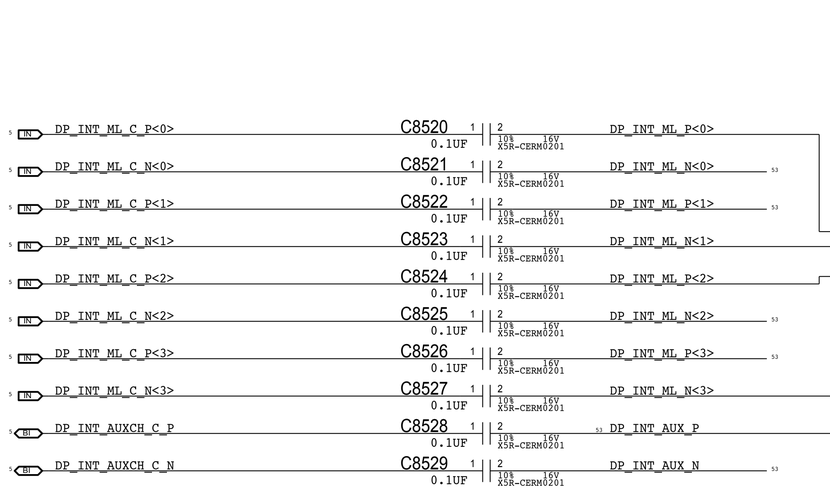
SHEET 52 OF 67

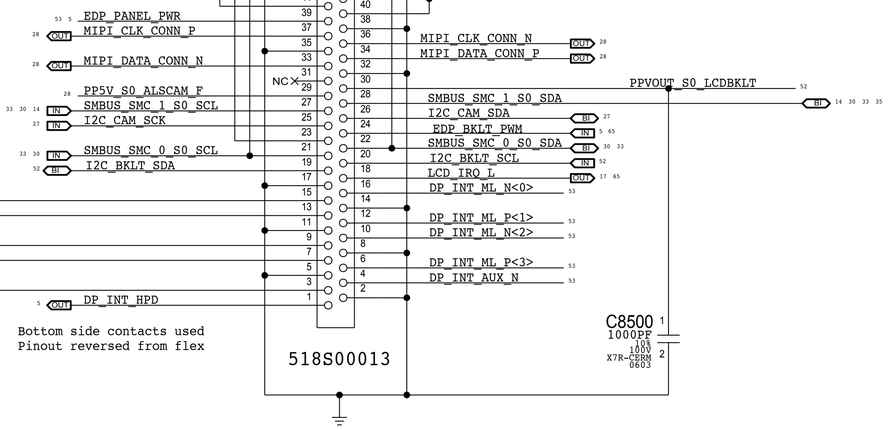
LCD PANEL INTERFACE (eDP) + Camera (MIPI)



U8320

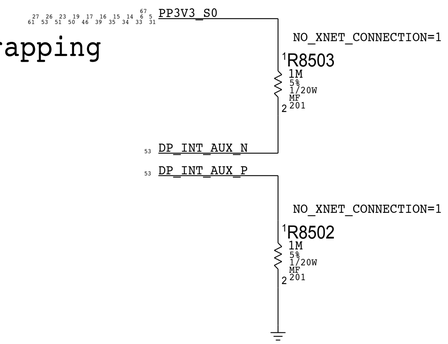
Part	TPS22904
Type	Load Switch
R(on) @ 2.5V	75 mOhm Typ 110 mOhm Max
Current	500mA Max





Bottom side contacts used
Pinout reversed from flex

LCD Panel HPD & AUX strapping



SYNC_MASTER=DEVMLB SYNC_DATE=05/11/2015

PAGE TITLE: eDP Display Connector

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 85 OF 130

SHEET: 53 OF 67

PRODUCT CAPACITY

CONFIG	CAPACITY2 R0864	CAPACITY1 R0863	CAPACITY0 R0862
000 - 32GB	NOSTUFF	NOSTUFF	NOSTUFF
001 - 64GB	NOSTUFF	NOSTUFF	ASSEMBLE
010 - 128GB	NOSTUFF	ASSEMBLE	NOSTUFF
011 - 256GB	NOSTUFF	ASSEMBLE	ASSEMBLE
100 - 512GB	ASSEMBLE	NOSTUFF	NOSTUFF
101 - 1024GB	ASSEMBLE	NOSTUFF	ASSEMBLE
110 - 2048GB	ASSEMBLE	ASSEMBLE	NOSTUFF
111 - RESERVED	ASSEMBLE	ASSEMBLE	ASSEMBLE

OPERATION MODE (ODT, CLK FREQ, ETC)

CONFIG	OP_MODE2 R8614	OP_MODE1 R8615	OP_MODE0 R8680
000 - TEABERRY	NOSTUFF	NOSTUFF	NOSTUFF
001 - XB58 GS	NOSTUFF	NOSTUFF	ASSEMBLE
010 - RESERVED	NOSTUFF	ASSEMBLE	NOSTUFF
011 - X260	NOSTUFF	ASSEMBLE	ASSEMBLE
100 - RESERVED	ASSEMBLE	NOSTUFF	NOSTUFF
101 - RESERVED	ASSEMBLE	NOSTUFF	ASSEMBLE
110 - RESERVED	ASSEMBLE	ASSEMBLE	NOSTUFF
111 - RESERVED	ASSEMBLE	ASSEMBLE	ASSEMBLE

OMIT_TABLE

U8600
S3X
BGA
SYM 3 OF 7

TP_S3X_DT0 — F18 DTO0
TP_S3X_DT1 — G18 DTO1

R8678 0 5% 1/20W MF 201 — S3X_XI — AK18 XI0 / AJ18 XO0

ANI03_ZQ — R8605 34.8 1% 1/20W MF 201 — R8603 3.01K 1% 1/20W MF 201 — S3X_PCIE_REF — H17 REXT

R8615 10K 5% 1/32W MF 01005 (PP1V8_S0SW_SSD_COLD)

NC T26 ANI03_ZQ_PD
T25 ANI03_ZQ_PU
T5 ANI47_ZQ_PD
T6 ANI47_ZQ_PU
S3X_GPIO0 — AD11 GPIO0
AD10 GPIO1
S3X_PFN — AE11 GPIO2

C8657 0.01UF 10% 10V X7R-CERM 0201 — PP1V8_S0SW_SSD_COLD (18 54 55 57 58 59 61)
C8658 0.01UF 10% 10V X7R-CERM 0201 — PP1V8_S0SW_SSD_COLD
ANI01_VREF (50)
ANI23_VREF (50)
C8650 0.01UF 10% 10V X7R-CERM 0201
C8652 0.01UF 10% 10V X7R-CERM 0201

REFCLK_P A19 PCIE_CLK100M_SSD_P (IN 16 63 65)
REFCLK_M A18 PCIE_CLK100M_SSD_N (IN 16 63 65)
PCIE_TX0_P A17 PCIE_SSD_D2R_C_P<0>
PCIE_TX0_M A16 PCIE_SSD_D2R_C_N<0>
PCIE_TX1_P A15 PCIE_SSD_D2R_C_P<1>
PCIE_TX1_M A14 PCIE_SSD_D2R_C_N<1>
PCIE_TX2_P A13 NC_PCIE_SSD_D2R_CP<2> (OUT 63)
PCIE_TX2_M A12 NC_PCIE_SSD_D2R_CN<2> (OUT 63)
PCIE_TX3_P A11 NC_PCIE_SSD_D2R_CP<3> (OUT 63)
PCIE_TX3_M A10 NC_PCIE_SSD_D2R_CN<3> (OUT 63)
PCIE_RX0_P C17 =PCIE_SSD_R2D_P<0> (IN 63)
PCIE_RX0_M C16 =PCIE_SSD_R2D_N<0> (IN 63)
PCIE_RX1_P C15 =PCIE_SSD_R2D_P<1> (IN 63)
PCIE_RX1_M C14 =PCIE_SSD_R2D_N<1> (IN 63)
PCIE_RX2_P C13 NC_PCIE_SSD_R2DP<2> (IN 63)
PCIE_RX2_M C12 NC_PCIE_SSD_R2DN<2> (IN 63)
PCIE_RX3_P C11 NC_PCIE_SSD_R2DP<3> (IN 63)
PCIE_RX3_M C10 NC_PCIE_SSD_R2DN<3> (IN 63)
DDR_ATO J21 TP_S3X_DDR_ATO
BOOT_FROM_LPSR AF17 S3X_COLD_BOOT_L (IN 59)
CLK_IN AG18 SYSCLK_CLK24M_SSD (IN 18 65)
CLK_IN_SEL AD17 S3X_CLK_IN_SEL
PCIE_ATB0 G16 TP_S3X_PCIE_ATB0
PCIE_ATB1 G17 TP_S3X_PCIE_ATB1
PCIE_CLKREQ* F12 S3X_PCIE_CLKREQ_L (BI 59)
JTAG_TRST* AE18 TP_S3X_JTAG_TRST_L
RESET* AF18 S3X_RESET_L (IN 59)
HOLD_RESET AH18 S3X_HOLD_RESET
PERST* E12 S3X_PERST_L (IN 59)
JTAG_SEL AG20 S3X_JTAG_SEL — R8624 10K 5% 1/32W MF 01005
JTAG_TCK AH19 S3X_JTAG_TCK (IN 63 24)
JTAG_TDI AH17 TP_S3X_JTAG_TDI
JTAG_TDO AD20 TP_S3X_JTAG_TDO
JTAG_TMS AF19 S3X_JTAG_TMS (BI 23 24 63)
I2C_SCL E8 S3X_I2C_SCL (OUT 57 59)
I2C_SDA F8 S3X_I2C_SDA (BI 57 59)
PMIC_CTRL0 AF20 S3X_PMIC_CTRL0 (61 59 58 57 55 54 18 54 59)
PMIC_CTRL1 AE20 S3X_PMIC_CTRL1 (59)
PMIC_CTRL2 AG17 TP_S3X_PMIC_CTRL2
PMIC_EXT_CLK_DIS AH20 S3X_PMIC_EXT_CLK_DIS (59)
PMIC_LOW_PWR AD21 S3X_PMIC_LOW_PWR (59)
RET_LPSR_CLEAR AE17 S3X_RET_LPSR_CLEAR (59)
SPI_CLK F11 S3X_SPI_CLK
SPI_CS* G12 SSD_BOOT_L (IN 17 65)
SPI_MISO E11 NC
SPI_MOSI G10 NC
SPI_NOR_CLK E9 NC
SPI_NOR_CS* G11 NC
SPI_NOR_SIO0 H10 NC
SPI_NOR_SO1 C8 S3X_BOOTSTRAP3
SPI_NOR_SO2 F10 S3X_BOOTSTRAP4
SPI_NOR_SO3 G9 S3X_BOOTSTRAP5
SPI_NOR_RFN E10 NC
UART0_RX B8 S3X_SMC_OOB_UART_R2D (59)
UART0_TX A8 (59) S3X_SMC_OOB_UART_D2R
UART1_RX B7 S3X_DEBUG_UART_R2D
UART1_TX A7 S3X_DEBUG_UART_D2R (OUT 59)
RETEN_EN H18 S3X_RET_EN_L (IN 59)
DDR_PHY_DATA_VREF AD12 S3X_DDR_PHY_DATA_VREF
DDR_PHY_ZQ G21 S3X_DDR_PHY_ZQ
DDR_VREFI_ALIVE B23 S3X_DDR_VREFI_ALIVE
DDR_VREFI_ZQ J20 S3X_DDR_VREFI_ZQ
DDR_VREFO AH16 S3X_DDR_VREFO
DDR_ZQ B26 S3X_DDR_ZQ
DDR_CKE0 C20 S3X_DDR_CKE0
DDR_CKE1 C21 S3X_DDR_CKE1

GND_VOID=TRUE C8610 0.22UF GND_VOID=TRUE =PCIE_SSD_D2R_P<0> (OUT 63)
GND_VOID=TRUE C8611 0.22UF GND_VOID=TRUE =PCIE_SSD_D2R_N<0> (OUT 63)
GND_VOID=TRUE C8613 0.22UF GND_VOID=TRUE =PCIE_SSD_D2R_P<1> (OUT 63)
GND_VOID=TRUE C8612 0.22UF GND_VOID=TRUE =PCIE_SSD_D2R_N<1> (OUT 63)
GND_VOID=TRUE C8614 0.22UF GND_VOID=TRUE PCIE_SSD_R2D_P<0> (OUT 63) — PCIE_SSD_R2D_C_P<0> (IN 16)
GND_VOID=TRUE C8615 0.22UF GND_VOID=TRUE PCIE_SSD_R2D_N<0> (OUT 63) — PCIE_SSD_R2D_C_N<0> (IN 16)
GND_VOID=TRUE C8617 0.22UF GND_VOID=TRUE PCIE_SSD_R2D_P<1> (OUT 63) — PCIE_SSD_R2D_C_P<1> (IN 16)
GND_VOID=TRUE C8616 0.22UF GND_VOID=TRUE PCIE_SSD_R2D_N<1> (OUT 63) — PCIE_SSD_R2D_C_N<1> (IN 16)

PP1V8_S0SW_SSD_COLD (61 59 58 57 55 54 18)
R8604 100K 5% 1/20W MF 201
R8676 10K 5% 1/32W MF 01005
R8677 10K 5% 1/32W MF 01005
R8674 0 5% 1/20W MF 201

R8612 10K 5% 1/32W MF 01005
R8629 10K 5% 1/32W MF 01005
R8673 10K 5% 1/32W MF 01005 (IN 59 63) — PP1V8_S0SW_SSD_COLD (18 54 55 57 58 59 61)

PP1V8_S0SW_SSD_COLD (18 54 55 57 58 59 61)
R8680 10K 5% 1/32W MF 01005
S3X_PMIC_CTRL0 (59 54)

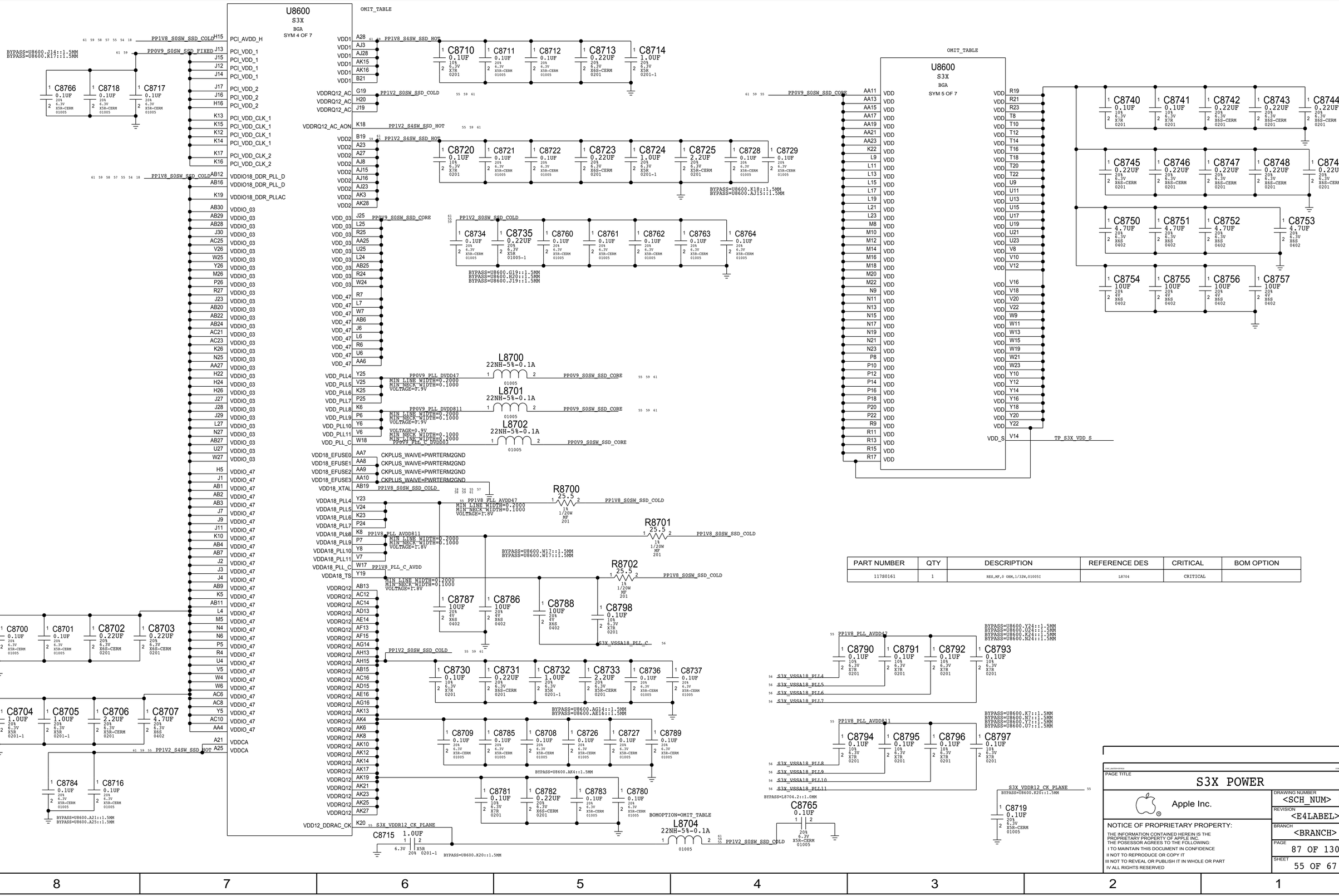
PP1V8_S0SW_SSD_COLD (61 59 58 57 55 54 18)
SANDISK_1Y R8616 10K 5% 1/32W MF 01005
CAPACITY0 R8662 10K 5% 1/32W MF 01005
CAPACITY1 R8663 10K 5% 1/32W MF 01005
CAPACITY2 R8664 10K 5% 1/32W MF 01005

R8610 1.00K 5% 1/32W MF 01005 NOSTUFF
R8611 1.00K 5% 1/32W MF 01005 NOSTUFF
R8607 240 1% 1/20W MF 201
C8620 1000PF 10% 16V X7R-1 0201
C8621 1000PF 10% 16V X7R-1 0201
C8622 1000PF 10% 16V X7R-1 0201
C8623 1000PF 10% 16V X7R-1 0201
R8608 240 1% 1/20W MF 201 PACK_TYPE=201 — PLACE_NEAR=U8600.G21:3.0MM

PLACE_NEAR=U8600.B26:3.0MM
BYPASS=U8600.J20:±3.0MM
BYPASS=U8600.B23:±3.0MM
BYPASS=U8600.AH16:±3.0MM
BYPASS=U8600.AD12:±3.0MM

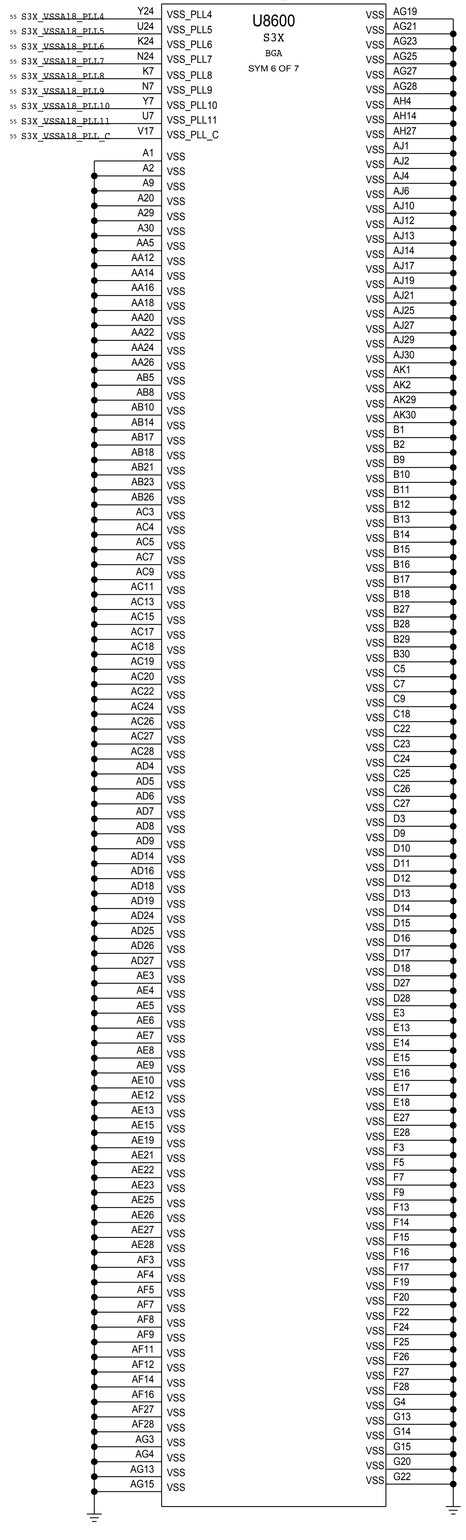
PAGE TITLE	S3X CORE, PCIE
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
	PAGE 86 OF 130
	SHEET 54 OF 67

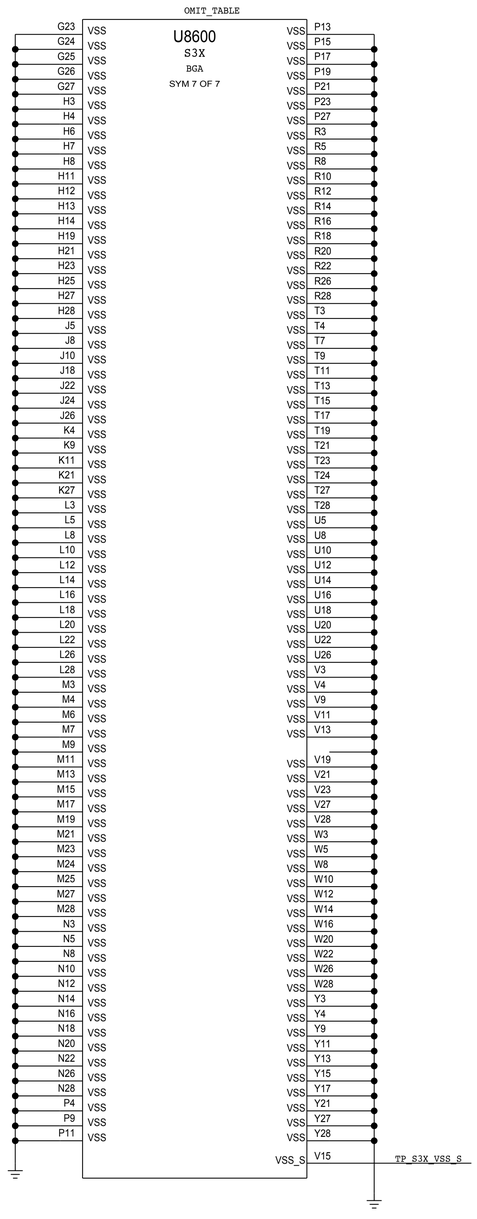
NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

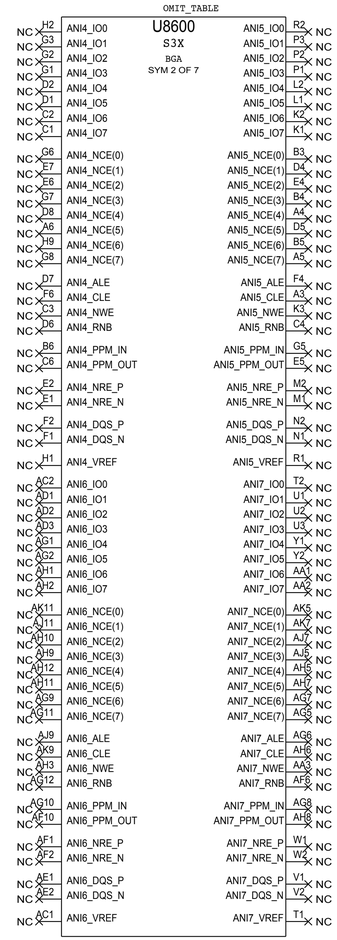


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0161	1	RES,MF,0 OHM,1/32W,01005!	L8704	CRITICAL	

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 87 OF 130
SHEET 55 OF 67







SYNC_MASTER=DEVMLB SYNC_DATE=05/11/2015

PAGE TITLE

S3X GND

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 88 OF 130

SHEET 56 OF 67

DEVICE 2-WIRE ADDRESS	ADD0 PIN CONNECTION
1001010	SDA

PLACE U9010 Opposite of S3X controller

61 59 58 55 54 18 PP1V8_S0SW_SSD_COLD

R9010 4.7K 5% 1/20W MF 201

R9011 4.7K 5% 1/20W MF 201

U9010 HPA00330AI SOT563

59 57 54 BI S3X_I2C_SDA

59 54 BI S3X_I2C_SCL

SDA SCL ADD0 ALERT GND V+ NC

C9010 0.01UF 10% 10V X5R-CERM 0201 BYPASS=U9010.5::3.0MM

61 59 58 57 PP3V3R2V7_NAND_VCC

R9003 10K 1% 1/20W MF 201

R9031 10K 0.1% 1/20W MF 0201-1

NO_XNET_CONNECTION=1

61 50 45 PP5V_S5

R9001 2.2 5% 1/20W MF 201

R9006 2.2 5% 1/20W MF 201

PP2V7_NAND_PVCC

MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2000
VOLTAGE=5V

C9021 10UF 20% 6.3V CERM-X6S 0402

PP2V7_NAND_VCC

MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2000
VOLTAGE=5V

C9022 2.2UF 10% 10V X6S-CERM 0402

U9000 ISL95870AH UTQFW CRITICAL

VCC PVCC

59 IN PICCOLO_VEN1

P2V7NAND_SENSE_DIV

P2V7NAND_SREF

P2V7NAND_VO

P2V7NAND_OCSET

59 OUT PICCOLO_POK1

P2V7NAND_RTN_DIV

P2V7NAND_SET0

P2V7NAND_SET1

GND PGND

EN FB SREF VO OCSET PGOOD RTN FSEL SET0 SET1 VID0 VID1

BOOT UGATE PHASE LGATE

61 59 52 46 45 41 34 29 PPBUS_G3H

P2V7NAND_BOOT_RC

MIN_LINE_WIDTH=0.3000
MIN_NECK_WIDTH=0.2000
DIDT=TRUE

C9016 0.1UF 10% 16V X7R-CERM 0402

R9009 2.2 5% 1/20W MF 201

P2V7NAND_VBST

MIN_LINE_WIDTH=0.3000
MIN_NECK_WIDTH=0.2000
DIDT=TRUE

P2V7NAND_DRVH_R

MIN_LINE_WIDTH=0.4000
MIN_NECK_WIDTH=0.2000
GATE_NODE=TRUE
DIDT=TRUE

R9039 0 5% 1/20W MF 0201

P2V7NAND_DRVH

MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2000
GATE_NODE=TRUE
DIDT=TRUE

P2V7NAND_LL

MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2000
SWITCH_NODE=TRUE
DIDT=TRUE

65 P2V7NAND_DRVL

MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2000
GATE_NODE=TRUE
DIDT=TRUE

CRITICAL Q9001 CSD58879Q3D Q3D

TG TGR BG VIN VSW PGND

C9003 33UF 20% 16V TANT CASE-B1S

C9002 33UF 20% 16V TANT CASE-B1S

C9000 2.2UF 20% 25V X5R-CERM 0402-1

C9001 2.2UF 20% 25V X5R-CERM 0402-1

P2V7NAND_SW_LL

MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2000
SWITCH_NODE=TRUE
DIDT=TRUE

CRITICAL L9000 0.68UH-20%-6.7A-0.0194OHM PIMS042T-SM

P2V7NAND_DRVR_R

MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2000
VOLTAGE=2.7V

CRITICAL R9030 0.003 1% 1/2W MF 0306

57 58 59 61 PP3V3R2V7_NAND_VCC

C9005 10UF 20% 10V X5R-CERM 0402-1

C9006 10UF 20% 10V X5R-CERM 0402-1

C9008 150UF 20% 6.3V POLY-TANT CASE-B3-SM

C9007 150UF 20% 6.3V POLY-TANT CASE-B3-SM

C9004 12PF 5% 25V NP0-C0G 0201

C9009 12PF 5% 25V NP0-C0G 0201

C9011 12PF 5% 25V NP0-C0G 0201

C9012 12PF 5% 25V NP0-C0G 0201

P2V7NAND_P

P2V7NAND_N

R9021 1.87K 1% 1/20W MF 201

NO_XNET_CONNECTION=1

C9070 2200PF 10% 25V CER-X7R 0201

R9072 1.87K 1% 1/20W MF 201

C9023 0.01UF 10% 10V X7R-CERM 0201

R9017 191K 0.1% 1/20W MF 0201

R9018 95.3K 0.1% 1/20W MF 0201

P2V7NAND_SET_R

R9000 7.5K 1% 1/20W MF 201

C9026 10PF 5% 50V C0G 0201

R9004 10K 1% 1/20W MF 201

R9002 10K 0.1% 1/20W MF 0201-1

C9015 10PF 5% 50V C0G 0201

XW9000 SM

P2V7NAND_AGND

MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2000
VOLTAGE=0V

PLACE_NEAR=U9000.3:1mm

Vout = 2.85V
Freq = 1 MHz
Max OCP = 6.54 A
Nom OCP = 5.3 A
Min OCP = 4.1 A

SYNC_MASTER=X260_KUMAR SYNC_DATE=06/16/2015

PAGE TITLE

NAND VR, I2C ROM, TEMP SENSORS

Apple Inc.

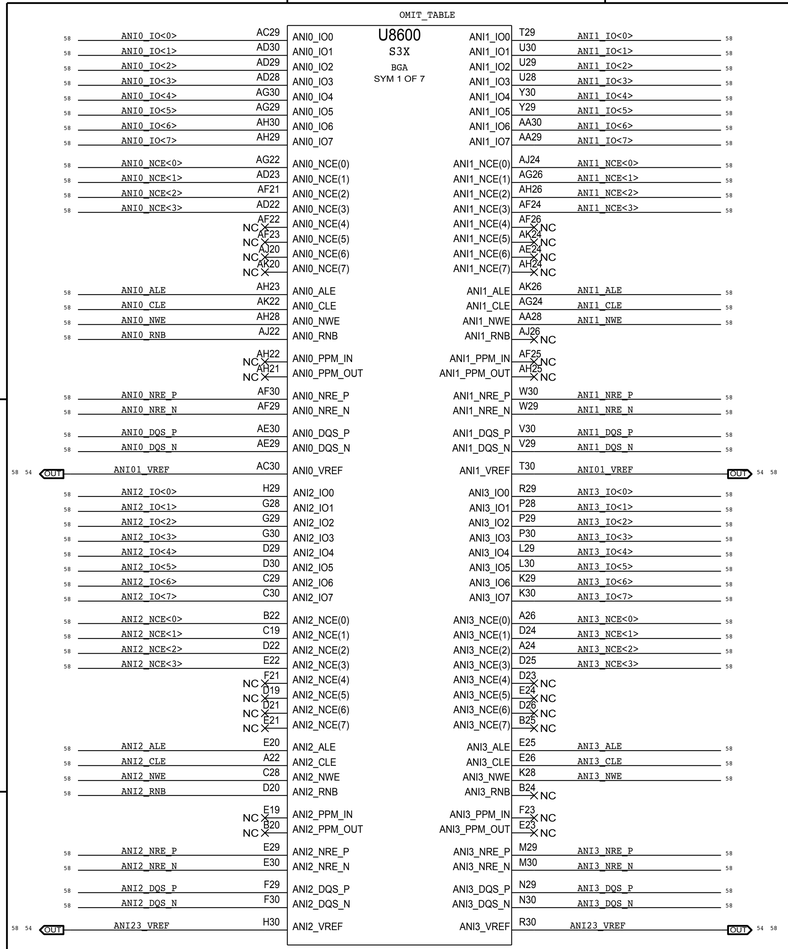
DRAWING NUMBER <SCH_NUM> SIZE D

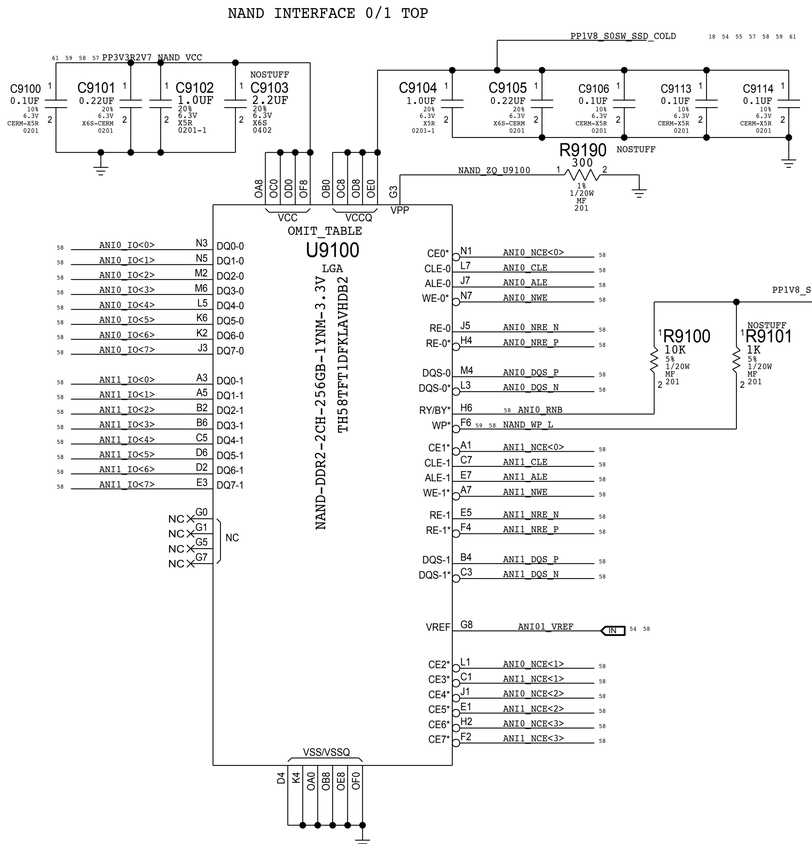
REVISION <E4LABEL>

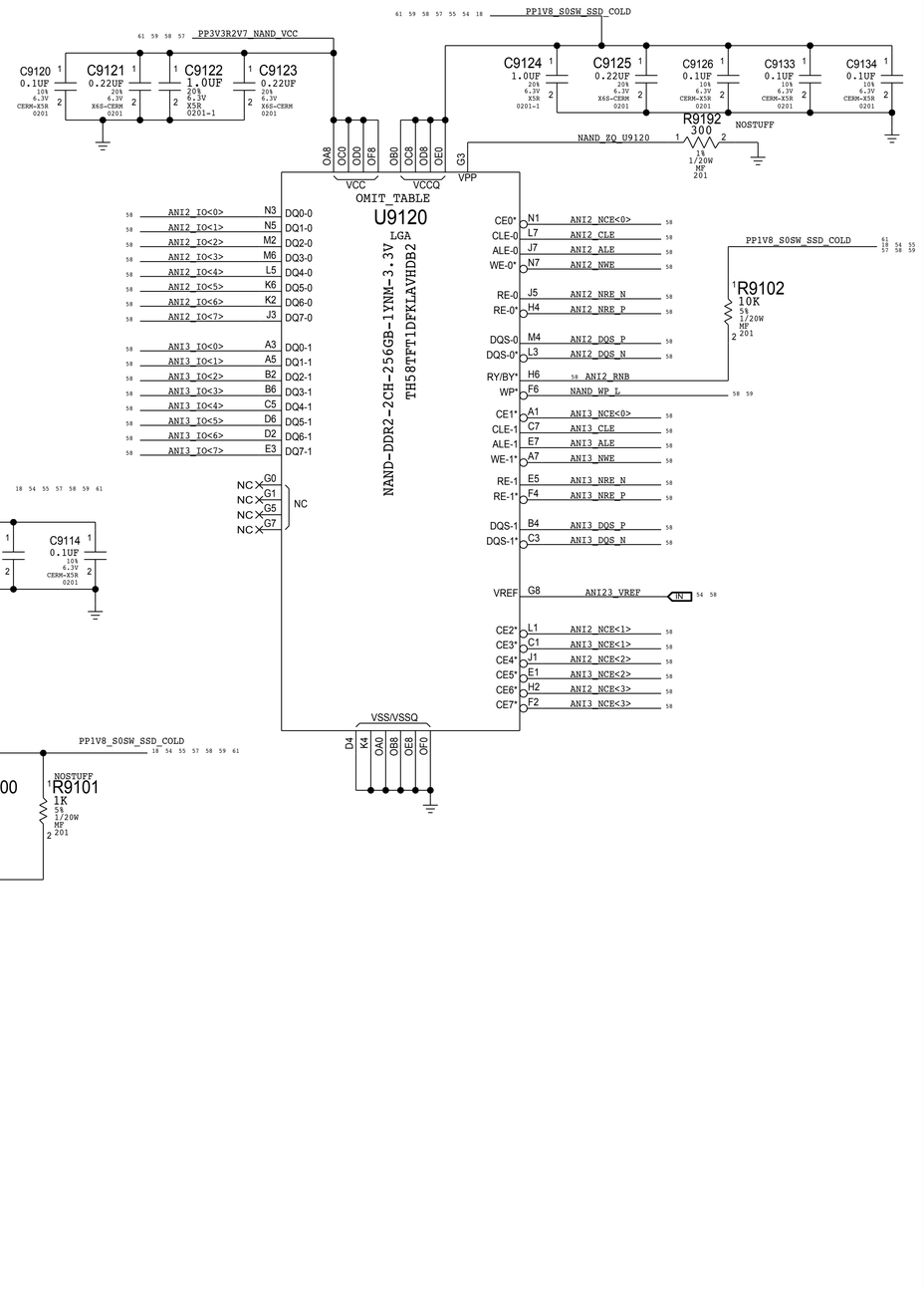
BRANCH <BRANCH>

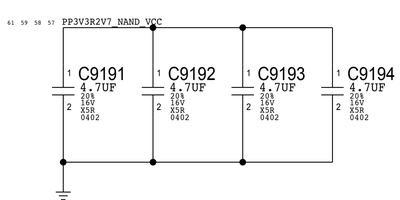
PAGE 90 OF 130

SHEET 57 OF 67









PAGE TITLE

NAND & ANI[3:0]

Apple Inc.

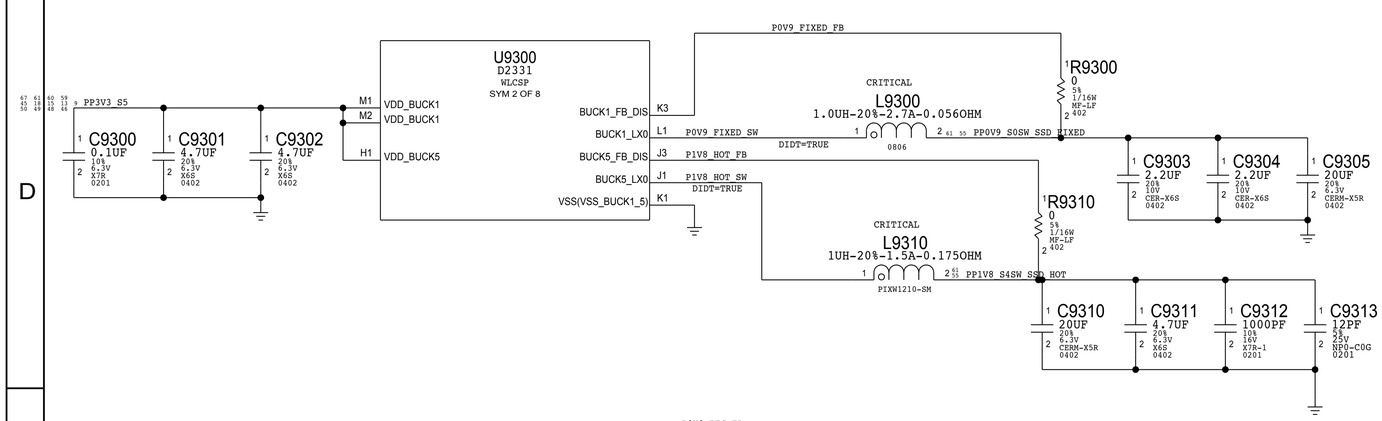
DRAWING NUMBER <SCH_NUM> | SIZE D

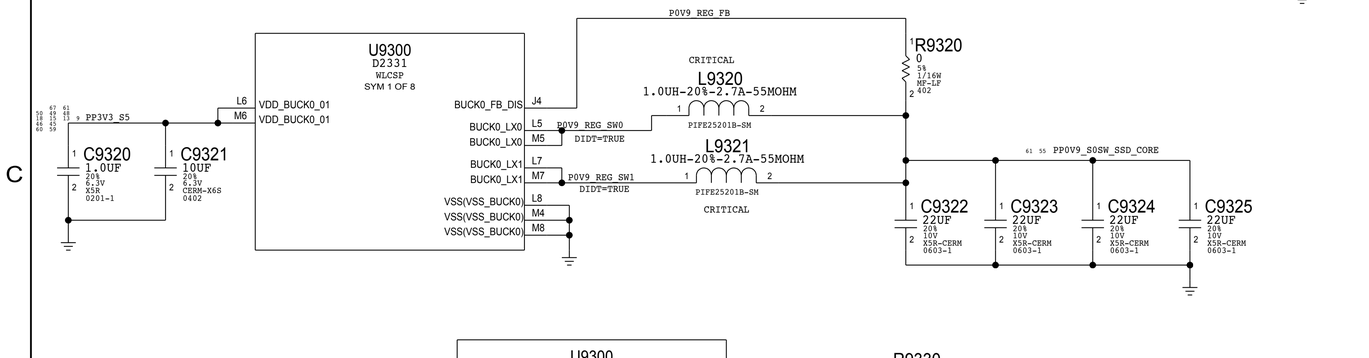
REVISION <E4LABEL>

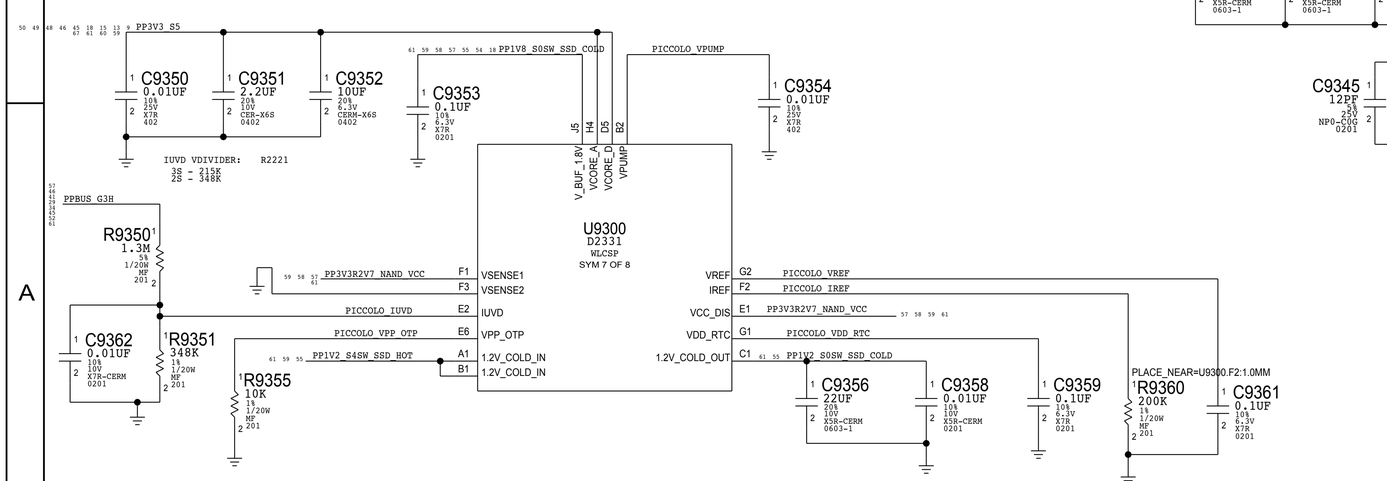
BRANCH <BRANCH>

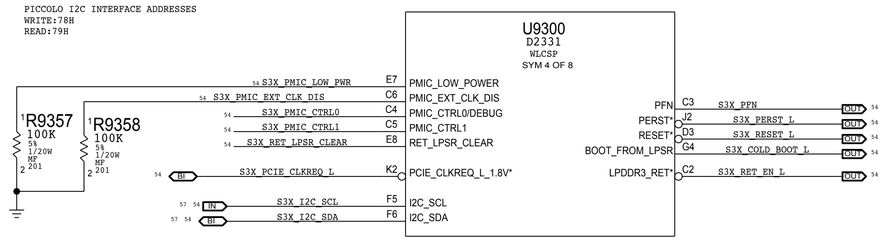
PAGE 91 OF 130

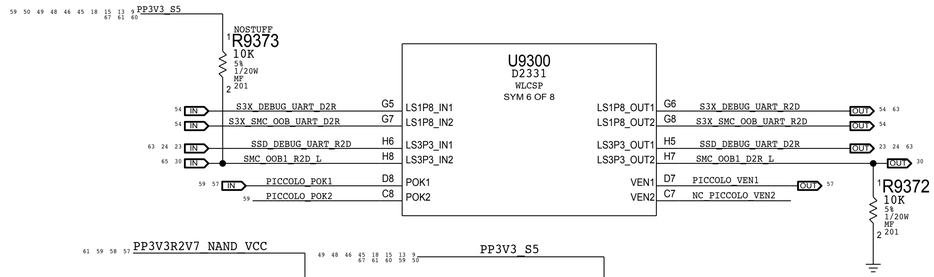
SHEET 58 OF 67

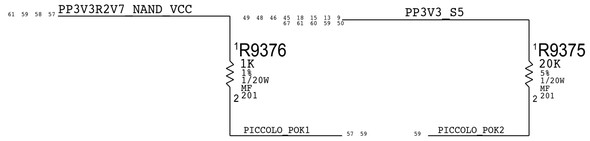


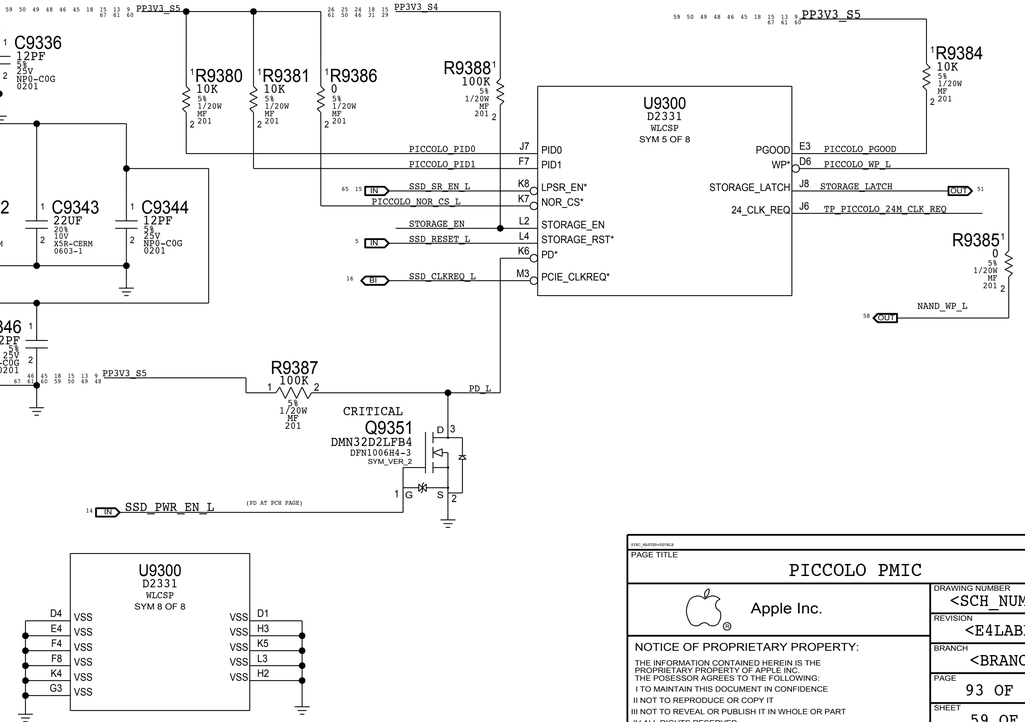






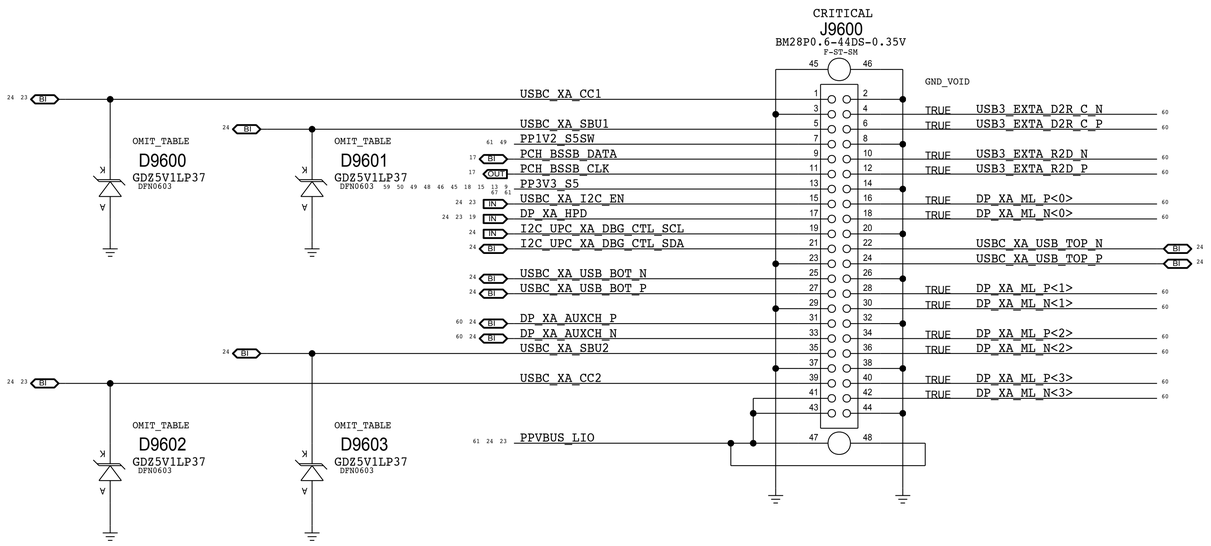






PAGE TITLE	PICCOLO PMIC
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
	PAGE 93 OF 130
	SHEET 59 OF 67

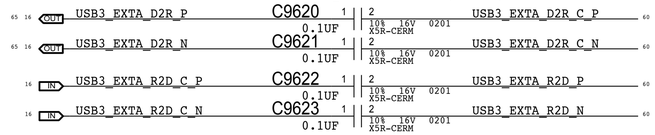
USB-C B2B RECEPTACLE
516S00038



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
371S00075	4	DIODE,ZENER,6.2V,250MW,DFN0603	D9600,D9601,D9602,D9603	CRITICAL	

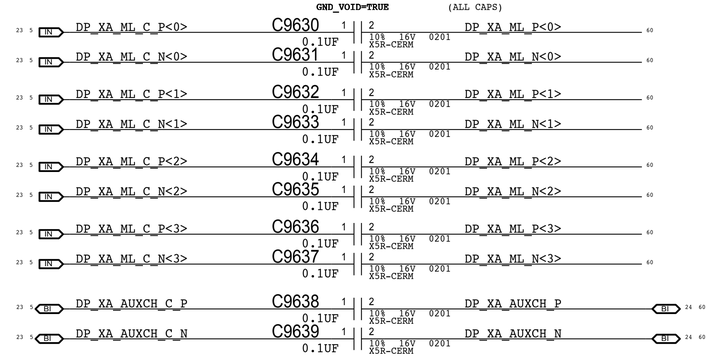
USB3 AC COUPLING

GND_VOID=TRUE (ALL CAPS)



DP SNK0 AC COUPLING

GND_VOID=TRUE (ALL CAPS)



SYNC_MASTER=DEVMLB SYNC_DATE=03/16/2015

PAGE TITLE

LIO Flex Connector

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 96 OF 130

SHEET 60 OF 67

"G3Hot" (Always-Present) Rails

PPBUS_G3H
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2000
VOLTAGE=8.6V
MAKE_BASE=TRUE

PPBUS_G3H
PPBUS_G3H
PPBUS_G3H
PPBUS_G3H
PPBUS_G3H
PPBUS_G3H
PPBUS_G3H
PPBUS_G3H

PPVIN_G3H_P3V3G3H
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2000
VOLTAGE=8.6V
MAKE_BASE=TRUE

PPBUS_S5_HS_COMPUTING_ISNS
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2000
VOLTAGE=8.6V
MAKE_BASE=TRUE

PPBUS_S5_HS_COMPUTING_ISNS
PPBUS_S5_HS_COMPUTING_ISNS
PPBUS_S5_HS_COMPUTING_ISNS
PPBUS_S5_HS_COMPUTING_ISNS
PPBUS_S5_HS_COMPUTING_ISNS

PPVBUS_LIO
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.1000
VOLTAGE=20V
MAKE_BASE=TRUE

PPDCIN_G3H
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2000
VOLTAGE=20V
MAKE_BASE=TRUE

PPDCIN_G3H
PPDCIN_G3H

PP3V3_G3H
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.2000
VOLTAGE=3.42V
MAKE_BASE=TRUE

PP3V3_G3H
PP3V3_G3H
PP3V3_G3H
PP3V3_G3H
PP3V3_G3H
PP3V3_G3H
PP3V3_G3H
PP3V3_G3H

PP3V3R3V0_AON
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.1000
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3R3V0_AON

PPVRTC_G3H
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2000
VOLTAGE=3V
MAKE_BASE=TRUE

PPVRTC_G3H

5V Rails

PP5V_G3H
MIN_LINE_WIDTH=0.5000
MIN_NECK_WIDTH=0.2000
VOLTAGE=5V
MAKE_BASE=TRUE

PP5V_G3H
PP5V_G3H
PP5V_G3H
PP5V_G3H

PP5V_S5
MIN_LINE_WIDTH=0.5000
MIN_NECK_WIDTH=0.2000
VOLTAGE=5V
MAKE_BASE=TRUE

PP5V_S5
PP5V_S5
PP5V_S5
PP5V_S5

PP5V_S0SW_LCD
MIN_LINE_WIDTH=0.5000
MIN_NECK_WIDTH=0.2000
VOLTAGE=5V
MAKE_BASE=TRUE

PP5V_S0SW_LCD

PP5V_S4
MIN_LINE_WIDTH=0.5000
MIN_NECK_WIDTH=0.2000
VOLTAGE=5V
MAKE_BASE=TRUE

PP5V_S4
PP5V_S4
PP5V_S4
PP5V_S4
PP5V_S4
PP5V_S4
PP5V_S4

PP5V_S0
MIN_LINE_WIDTH=0.5000
MIN_NECK_WIDTH=0.2000
VOLTAGE=5V
MAKE_BASE=TRUE

PP5V_S0
PP5V_S0
PP5V_S0
PP5V_S0

3.3V Rails

PP3V3_S5
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.1000
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3_S5
PP3V3_S5
PP3V3_S5
PP3V3_S5
PP3V3_S5
PP3V3_S5
PP3V3_S5
PP3V3_S5
PP3V3_S5
PP3V3_S5
PP3V3_S5
PP3V3_S5
PP3V3_S5

PP3V3_SUS
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.1000
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3_SUS
PP3V3_SUS
PP3V3_SUS
PP3V3_SUS
PP3V3_SUS
PP3V3_SUS
PP3V3_SUS
PP3V3_SUS
PP3V3_SUS
PP3V3_SUS
PP3V3_SUS
PP3V3_SUS
PP3V3_SUS

PP3V3_S4
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2000
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3_S4
PP3V3_S4
PP3V3_S4
PP3V3_S4
PP3V3_S4
PP3V3_S4
PP3V3_S4
PP3V3_S4

PP3V3_S0
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.1000
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3_S0
PP3V3_S0
PP3V3_S0
PP3V3_S0
PP3V3_S0
PP3V3_S0
PP3V3_S0
PP3V3_S0
PP3V3_S0
PP3V3_S0
PP3V3_S0
PP3V3_S0
PP3V3_S0
PP3V3_S0
PP3V3_S0
PP3V3_S0
PP3V3_S0
PP3V3_S0

1.8V Rails

PP1V8_SUS
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2000
VOLTAGE=1.8V
MAKE_BASE=TRUE

PP1V8_SUS
PP1V8_SUS
PP1V8_SUS
PP1V8_SUS

PP1V8_S3
MIN_LINE_WIDTH=0.5000
MIN_NECK_WIDTH=0.2000
VOLTAGE=1.8V
MAKE_BASE=TRUE

PP1V8_S3
PP1V8_S3
PP1V8_S3

PP1V5_S0
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2000
VOLTAGE=1.5V
MAKE_BASE=TRUE

PP1V5_S0
PP1V5_S0
PP1V5_S0
PP1V5_S0

1.2V Rails

PP1V2_S3
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.1500
VOLTAGE=1.2V
MAKE_BASE=TRUE

PP1V2_S3
PP1V2_S3
PP1V2_S3
PP1V2_S3
PP1V2_S3
PP1V2_S3

PP1V2_S0SW
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.1000
VOLTAGE=1.2V
MAKE_BASE=TRUE

PP1V2_S0SW

PP1V2_S5SW
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.1000
VOLTAGE=1.2V
MAKE_BASE=TRUE

PP1V2_S5SW

Chipset Rails

PP1V_SUS
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2000
VOLTAGE=1.0V
MAKE_BASE=TRUE

PP1V_SUS
PP1V_SUS
PP1V_SUS
PP1V_SUS
PP1V_SUS
PP1V_SUS
PP1V_SUS
PP1V_SUS
PP1V_SUS
PP1V_SUS
PP1V_SUS
PP1V_SUS
PP1V_SUS
PP1V_SUS
PP1V_SUS
PP1V_SUS
PP1V_SUS

PP1V_SUS
? mA

PP1V_SUSSW_HSIO
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2000
VOLTAGE=1.0V
MAKE_BASE=TRUE

PP1V_SUSSW_HSIO
PP1V_SUSSW_HSIO
PP1V_SUSSW_HSIO
PP1V_SUSSW_HSIO

PP1V_SUSSW_HSIO
? mA

PP1V_S3
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2000
VOLTAGE=1.0V
MAKE_BASE=TRUE

PP1V_S3
PP1V_S3
PP1V_S3
PP1V_S3

PP1V_S3
? mA

PP1V_S0SW
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2000
VOLTAGE=1.0V
MAKE_BASE=TRUE

PP1V_S0SW

PP1V_S0SW
? mA

PPVCCIO_S0
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2500
VOLTAGE=1.0V
MAKE_BASE=TRUE

PPVCCIO_S0
PPVCCIO_S0

PPVCCIO_S0
? mA

PPVCCSA_S0
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2000
VOLTAGE=1.0V
MAKE_BASE=TRUE

PPVCCSA_S0

PPVCCSA_S0
? mA

PPVCCSA_DDR_S0
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2000
VOLTAGE=1.0V
MAKE_BASE=TRUE

PPVCCSA_DDR_S0

PPVCCSA_DDR_S0
? mA

SSD Rails

PP3V3R2V7_NAND_VCC
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.1000
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3R2V7_NAND_VCC

PP1V8_S0SW_SSD_COLD
MIN_LINE_WIDTH=0.0950
MIN_NECK_WIDTH=0.2000
VOLTAGE=1.8V
MAKE_BASE=TRUE

PP1V8_S0SW_SSD_COLD
PP1V8_S0SW_SSD_COLD

PP1V2_S0SW_SSD_COLD
MIN_LINE_WIDTH=0.0950
MIN_NECK_WIDTH=0.2000
VOLTAGE=1.2V
MAKE_BASE=TRUE

PP1V2_S0SW_SSD_COLD

PP1V8_S4SW_SSD_HOT
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2000
VOLTAGE=1.8V
MAKE_BASE=TRUE

PP1V8_S4SW_SSD_HOT

PP1V2_S4SW_SSD_HOT
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2000
VOLTAGE=1.2V
MAKE_BASE=TRUE

PP1V2_S4SW_SSD_HOT

PP0V9_S0SW_SSD_CORE
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.1500
VOLTAGE=0.9V
MAKE_BASE=TRUE

PP0V9_S0SW_SSD_CORE

PP0V9_S0SW_SSD_FIXED
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.1500
VOLTAGE=0.9V
MAKE_BASE=TRUE

PP0V9_S0SW_SSD_FIXED

CPU "VCORE" RAILS

PPVCORE_S0_CPU
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.1000
VOLTAGE=1.8V
MAKE_BASE=TRUE

PPVCORE_S0_CPU
PPVCORE_S0_CPU

GT "VCORE" RAILS

PPVCORE_S0_GT
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.1000
VOLTAGE=1.8V
MAKE_BASE=TRUE

PPVCORE_S0_GT
PPVCORE_S0_GT

PCH "VCORE" RAILS

PPVCORE_SUS_PCH
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.1000
VOLTAGE=1.8V
MAKE_BASE=TRUE

PPVCORE_SUS_PCH

RA000
0
5%
1/20W
MF
0201

PP5V_S0
PP5V_S4RS0
MIN_LINE_WIDTH=0.5000
MIN_NECK_WIDTH=0.2000
VOLTAGE=5V
MAKE_BASE=TRUE

PP5V_S4RS0
PP5V_S4RS0
PP5V_S4RS0

RA001
0
5%
1/20W
MF
0201

PP5V_S4

NO STUFF

Digital Ground

GND
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
VOLTAGE=0V

SYNC_MASTER=X260_ERIC
SYNC_DATE=06/09/2015

PAGE TITLE

Power Aliases

Apple Inc.

DRAWING NUMBER <SCH_NUM>
SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 100 OF 130
SHEET 61 OF 67

Memory Bit/Byte Swizzle

MAKE_BASE

BI	MEM_A_DQ<39>	TRUE	MEM_A_DQ<39>
BI	MEM_A_DQ<37>	TRUE	MEM_A_DQ<37>
BI	MEM_A_DQ<33>	TRUE	MEM_A_DQ<33>
BI	MEM_A_DQ<36>	TRUE	MEM_A_DQ<36>
BI	MEM_A_DQ<38>	TRUE	MEM_A_DQ<38>
BI	MEM_A_DQ<34>	TRUE	MEM_A_DQ<34>
BI	MEM_A_DQ<32>	TRUE	MEM_A_DQ<32>
BI	MEM_A_DQ<35>	TRUE	MEM_A_DQ<35>
BI	MEM_A_DQ<47>	TRUE	MEM_A_DQ<47>
BI	MEM_A_DQ<46>	TRUE	MEM_A_DQ<46>
BI	MEM_A_DQ<42>	TRUE	MEM_A_DQ<42>
BI	MEM_A_DQ<41>	TRUE	MEM_A_DQ<41>
BI	MEM_A_DQ<43>	TRUE	MEM_A_DQ<43>
BI	MEM_A_DQ<45>	TRUE	MEM_A_DQ<45>
BI	MEM_A_DQ<40>	TRUE	MEM_A_DQ<40>
BI	MEM_A_DQ<44>	TRUE	MEM_A_DQ<44>
BI	MEM_A_DQ<52>	TRUE	MEM_A_DQ<52>
BI	MEM_A_DQ<51>	TRUE	MEM_A_DQ<51>
BI	MEM_A_DQ<55>	TRUE	MEM_A_DQ<55>
BI	MEM_A_DQ<54>	TRUE	MEM_A_DQ<54>
BI	MEM_A_DQ<53>	TRUE	MEM_A_DQ<53>
BI	MEM_A_DQ<48>	TRUE	MEM_A_DQ<48>
BI	MEM_A_DQ<50>	TRUE	MEM_A_DQ<50>
BI	MEM_A_DQ<49>	TRUE	MEM_A_DQ<49>
BI	MEM_A_DQ<57>	TRUE	MEM_A_DQ<57>
BI	MEM_A_DQ<62>	TRUE	MEM_A_DQ<62>
BI	MEM_A_DQ<60>	TRUE	MEM_A_DQ<60>
BI	MEM_A_DQ<63>	TRUE	MEM_A_DQ<63>
BI	MEM_A_DQ<59>	TRUE	MEM_A_DQ<59>
BI	MEM_A_DQ<56>	TRUE	MEM_A_DQ<56>
BI	MEM_A_DQ<61>	TRUE	MEM_A_DQ<61>
BI	MEM_A_DQ<58>	TRUE	MEM_A_DQ<58>
BI	MEM_A_DQ<6>	TRUE	MEM_A_DQ<6>
BI	MEM_A_DQ<7>	TRUE	MEM_A_DQ<7>
BI	MEM_A_DQ<2>	TRUE	MEM_A_DQ<2>
BI	MEM_A_DQ<3>	TRUE	MEM_A_DQ<3>
BI	MEM_A_DQ<1>	TRUE	MEM_A_DQ<1>
BI	MEM_A_DQ<4>	TRUE	MEM_A_DQ<4>
BI	MEM_A_DQ<5>	TRUE	MEM_A_DQ<5>
BI	MEM_A_DQ<0>	TRUE	MEM_A_DQ<0>
BI	MEM_A_DQ<8>	TRUE	MEM_A_DQ<8>
BI	MEM_A_DQ<12>	TRUE	MEM_A_DQ<12>
BI	MEM_A_DQ<9>	TRUE	MEM_A_DQ<9>
BI	MEM_A_DQ<14>	TRUE	MEM_A_DQ<14>
BI	MEM_A_DQ<11>	TRUE	MEM_A_DQ<11>
BI	MEM_A_DQ<15>	TRUE	MEM_A_DQ<15>
BI	MEM_A_DQ<13>	TRUE	MEM_A_DQ<13>
BI	MEM_A_DQ<10>	TRUE	MEM_A_DQ<10>
BI	MEM_A_DQ<20>	TRUE	MEM_A_DQ<20>
BI	MEM_A_DQ<19>	TRUE	MEM_A_DQ<19>
BI	MEM_A_DQ<16>	TRUE	MEM_A_DQ<16>
BI	MEM_A_DQ<17>	TRUE	MEM_A_DQ<17>
BI	MEM_A_DQ<22>	TRUE	MEM_A_DQ<22>
BI	MEM_A_DQ<18>	TRUE	MEM_A_DQ<18>
BI	MEM_A_DQ<21>	TRUE	MEM_A_DQ<21>
BI	MEM_A_DQ<23>	TRUE	MEM_A_DQ<23>
BI	MEM_A_DQ<24>	TRUE	MEM_A_DQ<24>
BI	MEM_A_DQ<30>	TRUE	MEM_A_DQ<30>
BI	MEM_A_DQ<27>	TRUE	MEM_A_DQ<27>
BI	MEM_A_DQ<26>	TRUE	MEM_A_DQ<26>
BI	MEM_A_DQ<28>	TRUE	MEM_A_DQ<28>
BI	MEM_A_DQ<31>	TRUE	MEM_A_DQ<31>
BI	MEM_A_DQ<25>	TRUE	MEM_A_DQ<25>
BI	MEM_A_DQ<29>	TRUE	MEM_A_DQ<29>
BI	MEM_A_DQS_P<4>	TRUE	MEM_A_DQS_P<4>
BI	MEM_A_DQS_N<4>	TRUE	MEM_A_DQS_N<4>
BI	MEM_A_DQS_P<5>	TRUE	MEM_A_DQS_P<5>
BI	MEM_A_DQS_N<5>	TRUE	MEM_A_DQS_N<5>
BI	MEM_A_DQS_P<6>	TRUE	MEM_A_DQS_P<6>
BI	MEM_A_DQS_N<6>	TRUE	MEM_A_DQS_N<6>
BI	MEM_A_DQS_P<7>	TRUE	MEM_A_DQS_P<7>
BI	MEM_A_DQS_N<7>	TRUE	MEM_A_DQS_N<7>
BI	MEM_A_DQS_P<0>	TRUE	MEM_A_DQS_P<0>
BI	MEM_A_DQS_N<0>	TRUE	MEM_A_DQS_N<0>
BI	MEM_A_DQS_P<1>	TRUE	MEM_A_DQS_P<1>
BI	MEM_A_DQS_N<1>	TRUE	MEM_A_DQS_N<1>
BI	MEM_A_DQS_P<2>	TRUE	MEM_A_DQS_P<2>
BI	MEM_A_DQS_N<2>	TRUE	MEM_A_DQS_N<2>
BI	MEM_A_DQS_P<3>	TRUE	MEM_A_DQS_P<3>
BI	MEM_A_DQS_N<3>	TRUE	MEM_A_DQS_N<3>

MAKE_BASE

BI	MEM_B_DQ<22>	TRUE	MEM_B_DQ<22>
BI	MEM_B_DQ<16>	TRUE	MEM_B_DQ<16>
BI	MEM_B_DQ<18>	TRUE	MEM_B_DQ<18>
BI	MEM_B_DQ<23>	TRUE	MEM_B_DQ<23>
BI	MEM_B_DQ<17>	TRUE	MEM_B_DQ<17>
BI	MEM_B_DQ<20>	TRUE	MEM_B_DQ<20>
BI	MEM_B_DQ<21>	TRUE	MEM_B_DQ<21>
BI	MEM_B_DQ<19>	TRUE	MEM_B_DQ<19>
BI	MEM_B_DQ<25>	TRUE	MEM_B_DQ<25>
BI	MEM_B_DQ<24>	TRUE	MEM_B_DQ<24>
BI	MEM_B_DQ<26>	TRUE	MEM_B_DQ<26>
BI	MEM_B_DQ<30>	TRUE	MEM_B_DQ<30>
BI	MEM_B_DQ<28>	TRUE	MEM_B_DQ<28>
BI	MEM_B_DQ<29>	TRUE	MEM_B_DQ<29>
BI	MEM_B_DQ<31>	TRUE	MEM_B_DQ<31>
BI	MEM_B_DQ<27>	TRUE	MEM_B_DQ<27>
BI	MEM_B_DQ<55>	TRUE	MEM_B_DQ<55>
BI	MEM_B_DQ<50>	TRUE	MEM_B_DQ<50>
BI	MEM_B_DQ<48>	TRUE	MEM_B_DQ<48>
BI	MEM_B_DQ<53>	TRUE	MEM_B_DQ<53>
BI	MEM_B_DQ<51>	TRUE	MEM_B_DQ<51>
BI	MEM_B_DQ<52>	TRUE	MEM_B_DQ<52>
BI	MEM_B_DQ<54>	TRUE	MEM_B_DQ<54>
BI	MEM_B_DQ<49>	TRUE	MEM_B_DQ<49>
BI	MEM_B_DQ<57>	TRUE	MEM_B_DQ<57>
BI	MEM_B_DQ<56>	TRUE	MEM_B_DQ<56>
BI	MEM_B_DQ<59>	TRUE	MEM_B_DQ<59>
BI	MEM_B_DQ<62>	TRUE	MEM_B_DQ<62>
BI	MEM_B_DQ<60>	TRUE	MEM_B_DQ<60>
BI	MEM_B_DQ<61>	TRUE	MEM_B_DQ<61>
BI	MEM_B_DQ<58>	TRUE	MEM_B_DQ<58>
BI	MEM_B_DQ<63>	TRUE	MEM_B_DQ<63>
BI	MEM_B_DQ<2>	TRUE	MEM_B_DQ<2>
BI	MEM_B_DQ<0>	TRUE	MEM_B_DQ<0>
BI	MEM_B_DQ<4>	TRUE	MEM_B_DQ<4>
BI	MEM_B_DQ<1>	TRUE	MEM_B_DQ<1>
BI	MEM_B_DQ<6>	TRUE	MEM_B_DQ<6>
BI	MEM_B_DQ<5>	TRUE	MEM_B_DQ<5>
BI	MEM_B_DQ<7>	TRUE	MEM_B_DQ<7>
BI	MEM_B_DQ<3>	TRUE	MEM_B_DQ<3>
BI	MEM_B_DQ<11>	TRUE	MEM_B_DQ<11>
BI	MEM_B_DQ<14>	TRUE	MEM_B_DQ<14>
BI	MEM_B_DQ<9>	TRUE	MEM_B_DQ<9>
BI	MEM_B_DQ<15>	TRUE	MEM_B_DQ<15>
BI	MEM_B_DQ<13>	TRUE	MEM_B_DQ<13>
BI	MEM_B_DQ<10>	TRUE	MEM_B_DQ<10>
BI	MEM_B_DQ<8>	TRUE	MEM_B_DQ<8>
BI	MEM_B_DQ<12>	TRUE	MEM_B_DQ<12>
BI	MEM_B_DQ<35>	TRUE	MEM_B_DQ<35>
BI	MEM_B_DQ<37>	TRUE	MEM_B_DQ<37>
BI	MEM_B_DQ<33>	TRUE	MEM_B_DQ<33>
BI	MEM_B_DQ<32>	TRUE	MEM_B_DQ<32>
BI	MEM_B_DQ<38>	TRUE	MEM_B_DQ<38>
BI	MEM_B_DQ<39>	TRUE	MEM_B_DQ<39>
BI	MEM_B_DQ<36>	TRUE	MEM_B_DQ<36>
BI	MEM_B_DQ<34>	TRUE	MEM_B_DQ<34>
BI	MEM_B_DQ<47>	TRUE	MEM_B_DQ<47>
BI	MEM_B_DQ<45>	TRUE	MEM_B_DQ<45>
BI	MEM_B_DQ<46>	TRUE	MEM_B_DQ<46>
BI	MEM_B_DQ<41>	TRUE	MEM_B_DQ<41>
BI	MEM_B_DQ<43>	TRUE	MEM_B_DQ<43>
BI	MEM_B_DQ<42>	TRUE	MEM_B_DQ<42>
BI	MEM_B_DQ<40>	TRUE	MEM_B_DQ<40>
BI	MEM_B_DQ<44>	TRUE	MEM_B_DQ<44>
BI	MEM_B_DQS_P<2>	TRUE	MEM_B_DQS_P<2>
BI	MEM_B_DQS_N<2>	TRUE	MEM_B_DQS_N<2>
BI	MEM_B_DQS_P<3>	TRUE	MEM_B_DQS_P<3>
BI	MEM_B_DQS_N<3>	TRUE	MEM_B_DQS_N<3>
BI	MEM_B_DQS_P<6>	TRUE	MEM_B_DQS_P<6>
BI	MEM_B_DQS_N<6>	TRUE	MEM_B_DQS_N<6>
BI	MEM_B_DQS_P<7>	TRUE	MEM_B_DQS_P<7>
BI	MEM_B_DQS_N<7>	TRUE	MEM_B_DQS_N<7>
BI	MEM_B_DQS_P<0>	TRUE	MEM_B_DQS_P<0>
BI	MEM_B_DQS_N<0>	TRUE	MEM_B_DQS_N<0>
BI	MEM_B_DQS_P<1>	TRUE	MEM_B_DQS_P<1>
BI	MEM_B_DQS_N<1>	TRUE	MEM_B_DQS_N<1>
BI	MEM_B_DQS_P<4>	TRUE	MEM_B_DQS_P<4>
BI	MEM_B_DQS_N<4>	TRUE	MEM_B_DQS_N<4>
BI	MEM_B_DQS_P<5>	TRUE	MEM_B_DQS_P<5>
BI	MEM_B_DQS_N<5>	TRUE	MEM_B_DQS_N<5>

SYNC_MASTER=DEVMLB SYNC_DATE=04/30/2015

PAGE TITLE

Memory Signal Swaps

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 102 OF 130

SHEET 62 OF 67

MAKE_BASE

63 46 42	CPU_VR_READY	TRUE		CPU_VR_READY	42 46 63
63 30 15	SMC_PCH_SUSWARN_L	TRUE		SMC_PCH_SUSWARN_L	15 30 63
63 30 15	SMC_PCH_SUSACK_L	TRUE		SMC_PCH_SUSACK_L	15 30 63
63 41 34 31 30 65	SMC_BC_ACOK	TRUE		SMC_BC_ACOK	30 31 34 41 63 65
65 24 23 16	XDP_USB_EXTA_OC_L	TRUE		USB_EXTA_OC_L	23
64 63 16	USB_EXTB_OC_L	TRUE		USB_EXTB_OC_L	16 63 64
63 46 30 15	PM_RSMRST_L	TRUE		PM_RSMRST_L	15 30 46 63

MAKE_BASE

	GND	TRUE		GND	
63 46 45	P5VS4_PGOOD	TRUE		P5VS4_PGOOD	45 46 63
42 38 37 63 62 61 60 59 58 57 56 55 54 53 50 46 45	PP5V_S4			PP5V_S4	24 29 37 38 42 45 46 50 53 61 63 67

54	=PCIE_SSD_R2D_P<1..0>	TRUE		PCIE_SSD_R2D_P<1..0>	54
54	=PCIE_SSD_R2D_N<1..0>	TRUE		PCIE_SSD_R2D_N<1..0>	54
	=PCIE_SSD_R2D_P<3..2>	TRUE	1	NC_PCIE_SSD_R2DP<3..2>	54
	=PCIE_SSD_R2D_N<3..2>	TRUE	1	NC_PCIE_SSD_R2DN<3..2>	54
	PCIE_SSD_R2D_C_P<3..2>	TRUE	1	NC_PCIE_SSD_R2D_CP<3..2>	16
	PCIE_SSD_R2D_C_N<3..2>	TRUE	1	NC_PCIE_SSD_R2D_CN<3..2>	16
54	=PCIE_SSD_D2R_P<1..0>	TRUE		PCIE_SSD_D2R_P<1..0>	16 65
54	=PCIE_SSD_D2R_N<1..0>	TRUE		PCIE_SSD_D2R_N<1..0>	16 65
	PCIE_SSD_D2R_C_P<3..2>	TRUE	1	NC_PCIE_SSD_D2R_CP<3..2>	54
	PCIE_SSD_D2R_C_N<3..2>	TRUE	1	NC_PCIE_SSD_D2R_CN<3..2>	54
	PCIE_SSD_D2R_P<3..2>	TRUE	1	NC_PCIE_SSD_D2RP<3..2>	16
	PCIE_SSD_D2R_N<3..2>	TRUE	1	NC_PCIE_SSD_D2RN<3..2>	16
65 63 54 16	PCIE_CLK100M_SSD_P	TRUE		PCIE_CLK100M_SSD_P	16 54 63 65
65 63 54 16	PCIE_CLK100M_SSD_N	TRUE		PCIE_CLK100M_SSD_N	16 54 63 65
63 59 54	S3X_DEBUG_UART_R2D	TRUE		S3X_DEBUG_UART_R2D	54 59 63
59 24 23	SSD_DEBUG_UART_R2D	TRUE		SSD_UART_R2D	17 65
59 24 23	SSD_DEBUG_UART_R2D	TRUE		SSD_UART_R2D	17 65
63 51 50 46 19	PM_SLP_S0S3_L	TRUE		PM_SLP_S0S3_L	19 46 50 51 63
50 47 46 30 15 63 51	PM_SLP_S4_L	TRUE		PM_SLP_S4_L	15 30 46 47 50 51 63
65 63 18 16	SYSCLK_CLK24M_PCH	TRUE		SYSCLK_CLK24M_PCH	16 18 63 65
63 16	NC_PCH_CLK24M_XTALOUT	TRUE		NC_PCH_CLK24M_XTALOUT	16 63
63 5	NC_PCH_DDPC_CTRLDATA	TRUE		NC_PCH_DDPC_CTRLDATA	5 63

MAKE_BASE

63 6	NC_CPU_CFG0	TRUE		NC_CPU_CFG0	6 63
63 6	NC_CPU_CFG1	TRUE		NC_CPU_CFG1	6 63
63 6	NC_CPU_CFG2	TRUE		NC_CPU_CFG2	6 63
63 6	TP_CPU_CFG3	TRUE		TP_CPU_CFG3	6 63
63 6	NC_CPU_CFG5	TRUE		NC_CPU_CFG5	6 63
63 6	NC_CPU_CFG6	TRUE		NC_CPU_CFG6	6 63
63 6	NC_CPU_CFG7	TRUE		NC_CPU_CFG7	6 63
63 6	NC_CPU_CFG8	TRUE		NC_CPU_CFG8	6 63
63 6	NC_CPU_CFG9	TRUE		NC_CPU_CFG9	6 63
63 6	NC_CPU_CFG10	TRUE		NC_CPU_CFG10	6 63
63 6	NC_CPU_CFG11	TRUE		NC_CPU_CFG11	6 63
63 6	NC_CPU_CFG12	TRUE		NC_CPU_CFG12	6 63
63 6	NC_CPU_CFG13	TRUE		NC_CPU_CFG13	6 63
63 6	NC_CPU_CFG14	TRUE		NC_CPU_CFG14	6 63
63 6	NC_CPU_CFG15	TRUE		NC_CPU_CFG15	6 63
63 6	NC_CPU_CFG16	TRUE		NC_CPU_CFG16	6 63
63 6	NC_CPU_CFG17	TRUE		NC_CPU_CFG17	6 63
63 6	NC_CPU_CFG18	TRUE		NC_CPU_CFG18	6 63
63 6	NC_CPU_CFG19	TRUE		NC_CPU_CFG19	6 63

63 6	XDP_BPM_L<3..0>	TRUE		TP_XDP_BPM_L<3..0>	6
63 16	TP_XDP_CPU_PRDY_L	TRUE		TP_XDP_CPU_PRDY_L	16 63
63 16	TP_XDP_CPU_PREQ_L	TRUE		TP_XDP_CPU_PREQ_L	16 63
63 6	XDP_CPUPCH_TCK	TRUE		XDP_CPUPCH_TCK	6 63
63 6	XDP_CPUPCH_TDI	TRUE		XDP_CPUPCH_TDI	6 63
63 6	XDP_CPUPCH_TDO	TRUE	63 6	XDP_CPUPCH_TDO	
63 6	XDP_CPUPCH_TMS	TRUE		XDP_CPUPCH_TMS	6 63
63 6	XDP_CPUPCH_TRST_L	TRUE		XDP_CPUPCH_TRST_L	6 63
63 16	TP_XDP_PCH_OBSDATA_A2	TRUE		TP_XDP_PCH_OBSDATA_A2	16 63
63 6	TP_XDP_PCH_OBSDATA_A3	TRUE		TP_XDP_PCH_OBSDATA_A3	6 63
63 16	TP_XDP_PCH_OBSDATA_B0	TRUE		TP_XDP_PCH_OBSDATA_B0	16 63
63 14	TP_XDP_PCH_OBSDATA_C0	TRUE		TP_XDP_PCH_OBSDATA_C0	14 63
63 14	TP_XDP_PCH_OBSDATA_C1	TRUE		TP_XDP_PCH_OBSDATA_C1	14 63
63 14	TP_XDP_PCH_OBSDATA_C2	TRUE		TP_XDP_PCH_OBSDATA_C2	14 63
63 14	TP_XDP_PCH_OBSDATA_C3	TRUE		TP_XDP_PCH_OBSDATA_C3	14 63
63 14	TP_XDP_PCH_OBSDATA_D0	TRUE		TP_XDP_PCH_OBSDATA_D0	14 63
63 16	TP_XDP_PCH_OBSDATA_D1	TRUE		TP_XDP_PCH_OBSDATA_D1	16 63
63 16	TP_XDP_PCH_OBSDATA_D2	TRUE		TP_XDP_PCH_OBSDATA_D2	16 63
63 16	TP_XDP_PCH_OBSDATA_D3	TRUE		TP_XDP_PCH_OBSDATA_D3	16 63
63 6	TP_XDP_PCH_OBSFN_C1	TRUE		TP_XDP_PCH_OBSFN_C1	6 63
63 6	TP_XDP_PCH_TCK	TRUE		TP_XDP_PCH_TCK	6 63
63 6	XDP_CPUPCH_TDI	TRUE		XDP_CPUPCH_TDI	6 63
63 6	XDP_CPUPCH_TDO	TRUE		XDP_CPUPCH_TDO	6 63
63 6	XDP_CPUPCH_TMS	TRUE		XDP_CPUPCH_TMS	6 63
63 6	XDP_CPUPCH_TRST_L	TRUE		XDP_CPUPCH_TRST_L	6 63
63 6	XDP_CPUPCH_TCK	TRUE	63 6	XDP_CPUPCH_TCK	
63 6	TP_ITP_PMODE	TRUE		TP_ITP_PMODE	6 63
63 7	TP_CPU_MEMVTT_PWR_EN	TRUE		TP_CPU_MEMVTT_PWR_EN	7 63
63 30	TP_SMC_DEV_MLB	TRUE		TP_SMC_DEV_MLB	30 63
54 24 23	S3X_JTAG_TCK	TRUE		TP_S3X_JTAG_TCK	
54 24 23	S3X_JTAG_TMS	TRUE		TP_S3X_JTAG_TMS	

61 50 12 8 6 PP1V_S0SW

RA300 51 1 2 5% 1/20W MF 201

RA301 51 1 2 5% 1/20W MF 201

63 30	TP_SMC_DEBUGPRT_EN_L	TRUE		TP_SMC_DEBUGPRT_EN_L	30 63
63 14	TP_SPKR_ID0	TRUE		TP_SPKR_ID0	14 63
63 14	TP_SPKR_ID1	TRUE		TP_SPKR_ID1	14 63

SYNC_MASTER=X260_ERIC SYNC_DATE=06/04/2015

PAGE TITLE

X260 Signal Aliases

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 103 OF 130

SHEET 63 OF 67

NO_TEST Nets

NO_TEST

64 14	NC_PCH_BT_I2S_CLK	TRUE	NC_PCH_BT_I2S_CLK	14 64	CPU/PCH
64 14	NC_PCH_BT_I2S_D2R	TRUE	NC_PCH_BT_I2S_D2R	14 64	
64 14	NC_PCH_BT_I2S_R2D	TRUE	NC_PCH_BT_I2S_R2D	14 64	
64 14	NC_PCH_BT_I2S_SYNC	TRUE	NC_PCH_BT_I2S_SYNC	14 64	
64 14	NC_HDA_SDIN1	TRUE	NC_HDA_SDIN1	14 64	
64 15	NC_PCI_PME_L	TRUE	NC_PCI_PME_L	15 64	
64 14	NC_CLINK_CLK	TRUE	NC_CLINK_CLK	14 64	
64 14	NC_CLINK_DATA	TRUE	NC_CLINK_DATA	14 64	
64 14	NC_CLINK_RESET_L	TRUE	NC_CLINK_RESET_L	14 64	
64 5	NC_DP_DDI2_AUXCH_CP	TRUE	NC_DP_DDI2_AUXCH_CP	5 64	
64 5	NC_DP_DDI2_AUXCH_CN	TRUE	NC_DP_DDI2_AUXCH_CN	5 64	
64 5	NC_DP_DDI2_ML_CP<0>	TRUE	NC_DP_DDI2_ML_CP<0>	5 64	
64 5	NC_DP_DDI2_ML_CN<0>	TRUE	NC_DP_DDI2_ML_CN<0>	5 64	
64 5	NC_DP_DDI2_ML_CP<1>	TRUE	NC_DP_DDI2_ML_CP<1>	5 64	
64 5	NC_DP_DDI2_ML_CN<1>	TRUE	NC_DP_DDI2_ML_CN<1>	5 64	
64 5	NC_DP_DDI2_ML_CP<2>	TRUE	NC_DP_DDI2_ML_CP<2>	5 64	
64 5	NC_DP_DDI2_ML_CN<2>	TRUE	NC_DP_DDI2_ML_CN<2>	5 64	
64 5	NC_DP_DDI2_ML_CP<3>	TRUE	NC_DP_DDI2_ML_CP<3>	5 64	
64 5	NC_DP_DDI2_ML_CN<3>	TRUE	NC_DP_DDI2_ML_CN<3>	5 64	
64 30	NC_TCON_BKLT_PWM	TRUE	NC_TCON_BKLT_PWM	30 64	SMC
64 30	NC_SMC_GFX_OVERTEMP	TRUE	NC_SMC_GFX_OVERTEMP	30 64	
64 30	NC_SMC_GFX_THROTTLE_L	TRUE	NC_SMC_GFX_THROTTLE_L	30 64	
64 30	NC_SMC_GFX_SELF_THROTTLE	TRUE	NC_SMC_GFX_SELF_THROTTLE	30 64	
64 30	NC_SMC_FAN_0_CTL	TRUE	NC_SMC_FAN_0_CTL	30 64	
64 30	NC_SMC_FAN_0_TACH	TRUE	NC_SMC_FAN_0_TACH	30 64	
64 30	NC_SMC_FAN_1_CTL	TRUE	NC_SMC_FAN_1_CTL	30 64	
64 30	NC_SMC_FAN_1_TACH	TRUE	NC_SMC_FAN_1_TACH	30 64	
64 30	NC_SYS_ONEWIRE	TRUE	NC_SYS_ONEWIRE	30 64	
64 30	NC_SMC_SOC_POR	TRUE	NC_SMC_SOC_POR	30 64	
64 30	NC_SMC_DP_HPD_L	TRUE	NC_SMC_DP_HPD_L	30 64	
64 30	NC_SPI_SMC_CLK	TRUE	NC_SPI_SMC_CLK	30 64	
64 30	NC_SPI_SMC_CS_L	TRUE	NC_SPI_SMC_CS_L	30 64	
64 30	NC_SPI_SMC_MISO	TRUE	NC_SPI_SMC_MISO	30 64	
64 30	NC_SPI_SMC_MOSI	TRUE	NC_SPI_SMC_MOSI	30 64	
64 30	NC_SMC_ACTUATOR_ACTIVE_L	TRUE	NC_SMC_ACTUATOR_ACTIVE_L	30 64	
64 30	NC_WIFI_DEBUGPRT_R2D_L	TRUE	NC_WIFI_DEBUGPRT_R2D_L	30 64	
64 30	NC_WIFI_DEBUGPRT_D2R_L	TRUE	NC_WIFI_DEBUGPRT_D2R_L	30 64	

Unused nets with offpage

(Nets with offpages not used on this project)

	CAM_SENSOR_WAKE_L	27	CPUCORE_ISNS1_P	OUT 43
1893	JTAG_ISP_TDO	5	CPUCORE_ISNS1_N	OUT 43
1890	TBT_POC_RESET	5	CPUCORE_ISNS2_P	OUT 43
1889	LCD_PSR_EN	17	CPUCORE_ISNS2_N	OUT 43
1888	TBT_X_PLUG_EVENT_L	17	CPUSA_ISNS_P	OUT 43
1887	TBT_T_PLUG_EVENT_L	17	CPUSA_ISNS_N	OUT 43
1886	TBT_X_PCI_RESET_L	14	CPUGT_ISNS1_P	OUT 44
1885	TBT_T_PCI_RESET_L	14	CPUGT_ISNS1_N	OUT 44
1884	TBT_X_CIO_PWR_EN	14	CPUGT_ISNS2_P	OUT 44
1883	TBT_T_CIO_PWR_EN	14	CPUGT_ISNS2_N	OUT 44
1882	TBT_X_USB_PWR_EN	14	SOC_UART_D2R	OUT 17
1881	TBT_T_USB_PWR_EN	14	SOC_UART_R2D	OUT 17
1880	BT_PWRRST_L	6	SOC_UART_CTS_L	OUT 17
1879	BT_TIMESTAMP	6	SOC_UART_RTS_L	OUT 17
1878	PCH_SWD_IO	17	CPU_CFG<4>	OUT 6
1877	PCH_SWD_MUX_SEL	17	DP_DDI2_HPD	IN 5
1876	SOC_WAKE_L	17	XDP_USB_EXTC_OC_L	IN 16
1875	PCH_SWD_CLK	17	XDP_USB_EXTD_OC_L	IN 16
1874	USB_EXTB_OC_L	16 63	XDP_JTAG_ISP_TCK	OUT 16
17	AUD_SPI_CS_L	OUT	XDP_JTAG_ISP_TDI	OUT 16
17	AUD_SPI_CLK	OUT		
17	AUD_SPI_MISO	IN		
17	AUD_SPI_MOSI	OUT		

SYNC_MASTER=J92_DEVMLB SYNC_DATE=07/08/2014

PAGE TITLE

Func Test / No Test

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 104 OF 130

SHEET 64 OF 67

EE Chaz Probe Points

PPA504	SMC_CBC_ON	30 41
PPA505	SMC_CHGR_INT_L	30 41
PPA506	MEM_A_CAA<0>	7 21
PPA507	MEM_A_CLK_P<0>	7 21
PPA508	MEM_A_CLK_N<0>	7 21
PPA509	MEM_A_CS_L<0>	7 21
PPA510	MEM_B_DQ<12>	7 22 62
PPA511	MEM_A_DQS_P<1>	7 21 62
PPA512	MEM_A_DQS_N<1>	7 21 62
PPA513	AP_DEV_WAKE	14 25
PPA514	AP_S0IX_WAKE_L	17 18
PPA515	AP_S0IX_WAKE_SEL	17 18
PPA517	MIPI_CLK_P	27 28
PPA518	MIPI_DATA_P	27 28
PPA519	PCH_BT_UART_D2R	17 26
PPA520	PCH_BT_UART_RTS_L	17 26
PPA522	PCIE_CAMERA_D2R_P	16 28
PPA523	PCIE_CLK100M_SSD_P	16 54 63
PPA529	AUD_PWR_EN	17 39
PPA530	BT_UART_RTS_L	25 26
PPA531	CAMERA_PWR_EN	14 27
PPA533	EDP_BKLT_PWM	5 53
PPA534	HDA_SDIN0	14 39
PPA537	LCD_IRQ_L	17 53
PPA538	MEM_CAM_A<8>	27 28
PPA539	MEM_CAM_CS_L	27 28
PPA543	MIPI_CLK_N	27 28
PPA544	MIPI_DATA_N	27 28
PPA545	PCH_BT_UART_CTS_L	17 26
PPA546	PCH_BT_UART_R2D	17 26
PPA548	PCIE_CAMERA_D2R_N	16 28
PPA549	PCIE_CLK100M_SSD_N	16 54 63
PPA551	PCIE_SSD_D2R_N<0>	16 63
PPA552	PCIE_SSD_D2R_P<0>	16 63
PPA560	SMC_BT_PWR_EN	25 30
PPA562	SMC_OOB1_R2D_L	30 59
PPA563	SMC_PROCHOT	30 31
PPA564	SMC_SENSOR_PWR_EN	30 32 34
PPA565	SMC_WAKE_SCI_L	15 30
PPA566	SMC_WIFI_PWR_EN	25 30
PPA567	AP_PCIE_WAKE_L	18 25
PPA569	SSD_SR_EN_L	15 59
PPA570	SYSCLK_CLK12M_SMC	18 30
PPA571	SYSCLK_CLK24M_SSD	18 54
PPA572	SYSCLK_CLK24M_CAMERA	18 27 65
PPA575	TPAD_SPI_CS_L	17 29
PPA576	TPAD_SPI_INT_L	17 29
PPA577	USB3_EXTA_D2R_N	16 60
PPA578	USB3_EXTA_D2R_P	16 60
PPA579	CPU_CATERR_L	6 30
PPA581	MEM_B_CS_L<1>	7 22
PPA582	MEM_B_CKE<1>	7 22
PPA583	MEM_B_CAB<1>	7 22
PPA584	MEM_B_CAA<2>	7 22
PPA587	MEM_B_CAA<3>	7 22
PPA594	XDP_USB_EXTA_OC_L	16 23 24 63
PPA596	USB_EXTA_P	16 23
PPA597	USB_EXTA_N	16 23
PPA598	PM_DSW_PWRGD	15 30
PPA500	AP_CLKREQ_L	16 25
PPA501	AP_RESET_L	14 25
PPA502	CAMERA_CLKREQ_L	16 27
PPA503	CAMERA_RESET_L	14 27
PPA521	CHGR_BOOST_DH	41
PPA586	CHGR_BOOST_DL	41
PPA524	CHGR_BUCK_DH	41
PPA525	CHGR_BUCK_DL	41
PPA526	CPUCORE_FCCM	42 43
PPA527	CPUGT_FCCM	42 44
PPA528	CPUSA_FCCM	42 43
PPA532	CPUCORE_PWM1	42 43
PPA535	CPUCORE_PWM2	42 43
PPA536	CPUGT_PWM1	42 44
PPA540	CPUGT_PWM2	42 44
PPA541	CPUSA_PWM	42 43
PPA542	P1V2_DRVH	47
PPA547	P1V2_DRVL	47
PPA589	PVCCIO_DRVH	47
PPA588	PVCCIO_DRVL	47
PPA550	P1VSUS_DRVH	48
PPA590	P1VSUS_DRVL	48
PPA553	LPC_SERIRQ	14 30
PPA554	SMC_CLK32K	30 31
PPA555	SYSCLK_CLK32K_PCH	16 18
PPA556	SYSCLK_CLK32K_CAMERA_BT_AP	18 25
PPA557	SYSCLK_CLK24M_PCH	16 18 63
PPA558	TPAD_SPI_IF_EN	17 29
PPA559	CPUCORE_GL1	43
PPA561	CPUCORE_GL2	43
PPA568	CPUGT_GL1	44
PPA573	CPUGT_GL2	44
PPA574	SMC_BC_ACOK	30 31 34 41 63
PPA580	P2V7NAND_DRVL	57
PPA585	P1V8SUS_PGOOD	46 48

SSD & WiFi Chamber Test Points

TPA500	PPDCIN_G3H	24 34 41 61 65
TPA501	PPDCIN_G3H	24 34 41 61 65
TPA502	PPDCIN_G3H	24 34 41 61 65
TPA503	PPDCIN_G3H	24 34 41 61 65
TPA504	GND	
TPA505	GND	
TPA506	SMC_ONOFF_L	29 30 31 32
TPA507	SSD_BOOT_L	17 54
TPA508	SMC_DEV_SUPPLY_L	30
TPA509	GND	
TPA510	SMC_DEBUGPRT_TX_L	30 31 65
TPA511	SMC_DEBUGPRT_RX_L	30 31 65
TPA512	SSD_UART_R2D	17 63
TPA513	SSD_UART_D2R	17 63
TPA514	PCIE_TEST_D2R_P	PCIE_TEST_D2R_P 16 65
TPA515	PCIE_TEST_D2R_N	PCIE_TEST_D2R_N 16 65
TPA516	PCIE_TEST_R2D_P	PCIE_TEST_R2D_P 16 65
TPA517	PCIE_TEST_R2D_N	PCIE_TEST_R2D_N 16 65
TPA518	PCIE_CLK100M_TEST_P	PCIE_CLK100M_TEST_P 16 65
TPA519	PCIE_CLK100M_TEST_N	PCIE_CLK100M_TEST_N 16 65
TPA520	TEST_CLKREQ_L	TEST_CLKREQ_L 16 65
TPA521	PLT_RST_L	5 14 15 19 26 30
TPA522	USB_TEST_P	USB_TEST_P 16 65
TPA523	USB_TEST_N	USB_TEST_N 16 65
TPA524	GND	
TPA525	GND	
TPA526	POWER_GATE_EN	23 24 41
TPA527	PP3V3R3V0_AON	23 41 61
TPA528	HIPWR_EN	23 41
TPA529	PM_SLP_S3_L	15 30 46 49 50 51

All TPA parts: A, SM-TPP635-TOP; PCIE_TEST_D2R_P, PCIE_TEST_D2R_N, PCIE_TEST_R2D_P, PCIE_TEST_R2D_N, PCIE_CLK100M_TEST_P, PCIE_CLK100M_TEST_N, TEST_CLKREQ_L, USB_TEST_P, USB_TEST_N: MAKE_BASE=TRUE

65 27 18 SYSCLK_CLK24M_CAMERA			SYSCLK_CLK24M_CAMERA 18 27 65
	MAKE_BASE=TRUE		
24 23 SMC_UART_TX		TRUE	SMC_DEBUGPRT_TX_L 30 31 65
24 23 SMC_UART_RX		TRUE	SMC_DEBUGPRT_RX_L 30 31 65

NO_TEST Nets

	NO_TEST MAKE_BASE		
65 16 NC_USB3_EXTB_D2RP		TRUE	NC_USB3_EXTB_D2RP 16 65
65 16 NC_USB3_EXTB_D2RN		TRUE	NC_USB3_EXTB_D2RN 16 65
65 16 NC_USB3_EXTB_R2D_CP		TRUE	NC_USB3_EXTB_R2D_CP 16 65
65 16 NC_USB3_EXTB_R2D_CN		TRUE	NC_USB3_EXTB_R2D_CN 16 65
65 16 NC_USB_EXTBP		TRUE	NC_USB_EXTBP 16 65
65 16 NC_USB_EXTBN		TRUE	NC_USB_EXTBN 16 65
65 16 NC_USB3_EXTC_D2RP		TRUE	NC_USB3_EXTC_D2RP 16 65
65 16 NC_USB3_EXTC_D2RN		TRUE	NC_USB3_EXTC_D2RN 16 65
65 16 NC_USB3_EXTC_R2D_CP		TRUE	NC_USB3_EXTC_R2D_CP 16 65
65 16 NC_USB3_EXTC_R2D_CN		TRUE	NC_USB3_EXTC_R2D_CN 16 65
65 16 NC_USB_EXTCP		TRUE	NC_USB_EXTCP 16 65
65 16 NC_USB_EXTCN		TRUE	NC_USB_EXTCN 16 65
65 16 NC_USB3_EXTD_D2RP		TRUE	NC_USB3_EXTD_D2RP 16 65
65 16 NC_USB3_EXTD_D2RN		TRUE	NC_USB3_EXTD_D2RN 16 65
65 16 NC_USB3_EXTD_R2D_CP		TRUE	NC_USB3_EXTD_R2D_CP 16 65
65 16 NC_USB3_EXTD_R2D_CN		TRUE	NC_USB3_EXTD_R2D_CN 16 65
65 16 NC_USB_EXTDP		TRUE	NC_USB_EXTDP 16 65
65 16 NC_USB_EXTDN		TRUE	NC_USB_EXTDN 16 65

CPU/PCH

SYNC_MASTER=J41_MLB SYNC_DATE=10/24/2012

PAGE TITLE: Project FCT/NC/Aliases

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 105 OF 130

SHEET: 65 OF 67

Reserved for Constraints!

Change List:

<radar://component/633819> X260 HW EE Schematic | Proto 0
<radar://component/634034> X260 HW EE Schematic | Proto 1
<radar://component/634038> X260 HW EE Schematic | Proto 2
<radar://component/634042> X260 HW EE Schematic | EVT
<radar://component/634046> X260 HW EE Schematic | DVT

Kismet:

<afp://kismet.apple.com/Kismet-Projects/>

Useful Wiki Links:

Schematic Conventions - <https://hmts.ecs.apple.com/wiki/index.php/User:Wferry/SchConventions>
Schematic Design Wiki - <https://hmts.ecs.apple.com/wiki/index.php/Schematic_Design>

Other Info:

Page Allocations - <radar:19817053> 2015 Mobile Mac Schematic Page Allocations

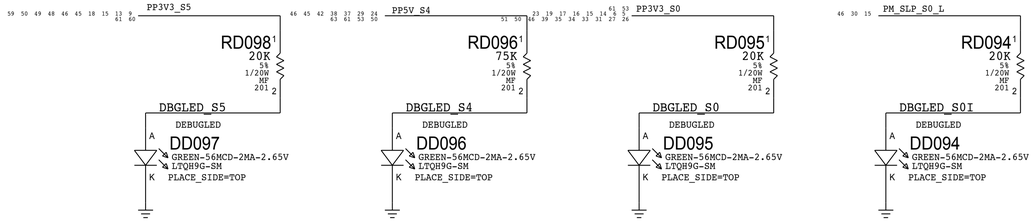
PAGE TITLE

Reference

Apple Inc.

DRAWING NUMBER <SCH_NUM>
SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>

Power State Debug LEDs



SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE

Debug Support

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 130 OF 130

SHEET 67 OF 67